



DELTA 2008

Fourth IEEE International Symposium on Electronic Design, Test and Applications

January 23-25, 2008
Hong Kong

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Message from General Chairs

It is our great pleasure and excitement to welcome you to the 2008 IEEE Symposium on Electronic Design, Test and Applications (DELTA 2008) that is taking place in the international city of Asia: Hong Kong. DELTA 2008 is the 4th in a series of very successful events organised under the auspices of Test Technology Technical Council of the IEEE Computer Society and in co-sponsorship and cooperation with other bodies. Its mission is to bring together scientists, engineers and researchers from all over the world to meet and discuss cutting-edge research, exchange innovative ideas and seek collaboration within and between academia and industry in rapidly growing areas of electronic design, test and applications.

The highlight of this year is the expansion of DELTA from an IEEE workshop to a full fledge IEEE symposium. This is a direct result of a healthy and steady progress of the event in terms of its significance, reputation, international exposure and diversity, as well as the quality and extent of its technical program reflected in terms of number of papers submitted and presented. This year has also witnessed a record submission (over 210 papers) and a high standard reflected in our acceptance rate of less than 42% for our regular papers.

Our program has always been flexible adapting to very fast changes in the electronic engineering field. This year, our sessions cover the latest advances in many new emerging areas such as biometric and security systems, FPGA and reconfigurable computing, advanced sensors design and implants, network and systems on chip, to name few. In addition DELTA 2008 is also

very delighted to host three authoritative keynote speakers from both academia (Prof. Niraj Jha of Princeton University and Prof. Charles Sodini of MIT) and industry (Dr. Stephen Lai, of Solomon Systech). Besides the solid technical program, the diversity of nationalities and topics that we were able to attract are very impressive indeed. DELTA is without any doubt progressively playing a key role and is becoming a superior event within IEEE in general and the design and test community in particular.

The quality of any symposium directly depends upon the selection process and the quality of the papers. Under the leadership of the program Co-Chairs Adam Osseiran, Abbas Amira and Michel Renovell, the program committee selected an outstanding set of papers. We would like to thank the Program Co-Chairs and all the TPC members for their expertise, hard work and dedication. We also thank all reviewers and authors who submitted papers and the speakers who will be presenting the papers: you are the real success holders of this symposium.

We are also grateful for our valuable sponsors: IEEE, TTTC of the IEEE Computer Society, Hong Kong University of Science and Technology, IEEE Hong Kong ED/SSC Joint Chapter. Additionally, we would like to thank our industrial sponsors and cooperating companies: Celoxica, Solomon Systech, National Instruments and Hong Kong Tourism board for their generous support to the Symposium.

Last but not least, we are confident the symposium will be highly productive and will provide participants with golden opportunities to make new contacts, meet new colleagues and refresh the existing network links as well as to discover and explore new ideas. We would like to encourage you to play a proactive role in the symposium and to contribute to this exciting event. We hope that you will find this symposium to be a technically rewarding experience. We do hope also that you will take this opportunity to explore Hong Kong. Above all, do enjoy DELTA 2008 and Hong Kong!



Amine Bermak,
General Co-Chair, DELTA 2008



Serge Demidenko,
General Co-Chair, DELTA 2008

Message from Technical Program Chairs

On behalf of the Program Committee of the 4th IEEE DELTA Symposium it is our pleasure to prepare for you this year's technical program.

DELTA has become one of the premier forums for presentation of new and exciting research in all aspects of electronic design, test and applications. These proceedings witness the progress of DELTA over time.

The papers in these proceedings were selected from a record total of 212 submissions; an unexpected increase from the previous DELTA 2006 that attracted 130 papers and 80 in DELTA 2004. This success is owed to the engineers, researchers and academics who recognised in DELTA a sufficiently successful technical meeting to entrust their work to.

The selected papers were chosen by a Program Committee of 55 world-class specialists in electronics fields such as analogue, digital and mixed-signal design and test, as well as numerous application areas related to advanced hardware and hardware-software electronic devices and systems. PC members were assisted by 43 external reviewers who altogether put in a major effort to complete more than 600 reviews in a record time.

The selection process started immediately after the submission deadline. Each paper was assigned to at least three program committee members and reviewers for appraisal. The papers were evaluated based on scientific originality, technical merit, and innovative contribution to the three fields of the Symposium. Final selection of the 87 papers and 33 posters that appear in these proceedings took place over several days.

On behalf of the Program Committee and Symposium as whole we would like to express our sincere thanks to the Program Committee

members, reviewers and special session organisers for their initiative, dedication, and hard work that have made possible this year's program.

We would like to thank all the authors who submitted papers. We sincerely hope they found the reviewers' comments helpful. We worked hard to make this event useful for advancement in your career in the current fast pace changing world of electronic technology. We sincerely hope that you will enjoy this symposium and find the technical program to be innovative, inspiring and rewarding.



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**Keynote 1: Wednesday 23<sup>rd</sup> Jan 2008,**  
**Lecture Theatre J, LTJ.**  
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**09:40-10:20 Professor Niraj K. Jha, EE
Department, Princeton
University, USA**
*"Digital System Testing: Emerging
Issues, Trends and Solution
Approaches"*

Abstract:

Advances in semiconductor and electronic design automation technology help continue the march to miniaturization of VLSI circuits. However, these increasing levels of integration present significant challenges to the developers of manufacturing-time tests. They put tremendous pressure on testing cost and time. This has led test engineers to constantly look for more efficient as well as accurate testing approaches.

Recently, satisfiability (SAT) solvers have made tremendous strides. Although SAT-based test generation has a 15-year old history, recent use of SAT for register-transfer level sequential test generation and design for testability has led to techniques that are both efficient and accurate. They can overcome several limiting assumptions hitherto made for RTL test generation that have prevented their use in the industrial setting. These limitations include the need for explicit controller/datapath separation, use of all test vectors or none from the pre-computed test set for any given module, dependence on symbolic justification (observability) paths from (to) circuit inputs (outputs) of a module, and a lack of applicability to mixed gate-level/RTL designs. We will discuss solution approaches that can overcome these limitations.

As CMOS technology approaches its physical limits, a tremendous amount of effort is being devoted to nanotechnology research in order to enable future technology scaling. Recent progress on various technologies, such as resonant tunneling diodes, quantum cellular automata, nanowires, nanotubes, single electron transistors, quantum computing, etc., points to promising directions for future circuit design. However, these technologies often use new logic primitives and thus necessitate newer fault models and test generation approaches. We will also discuss some emerging trends in this area.

About the Speaker:



Niraj K. Jha received his B.Tech. degree in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur, India in 1981 and Ph.D. degree in Electrical Engineering from University of Illinois at Urbana-Champaign in 1985. He is a Professor of Electrical Engineering at Princeton University. He is a Fellow of IEEE and ACM. He has served as the Director of the Center for Embedded System-on-a-chip Design funded by New Jersey Commission on Science and Technology. A textbook he co-authored titled "Testing of Digital Systems" is being used around the world.

He is the editor-in-chief of TVLSI and serves on the editorial boards of TCAD and TCAS. He has co-authored seven papers which have won Best Paper Awards. His research interests include nanotechnology, embedded system analysis and design, power/thermal aware hardware/software design, computer-aided design of ICs and systems, computer security, and digital system testing.

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**Keynote 2: Thursday 24<sup>th</sup> Jan 2008,**  
**Lecture Theatre J, LTJ.**  
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**15:20-16:00 Professor Charles Sodini, EECS
Department, Massachusetts
Institute of Technology, USA,**
*"System Drivers for Mixed Signal
Integrated Circuit Design Research"*

Abstract:

Mixed signal circuit design research is often carried out using design requirements that are determined by a system driver. One popular choice for system drivers is to use the latest evolving standards. However, these systems are often constrained and prevent the experimentation with novel circuit and system concepts. It has been our experience that the opportunity for innovation in mixed signal circuit design is enhanced when a system driver is conceived using state-of-the-art system concepts. An example of such a driver is the Wireless Gigabit Local Area Network (WiGLAN) that was used as a system driver for communication circuit research from 1998-2006. The WiGLAN offers Gb/s data rates in the 5GHz band using the concept of adaptive modulation of sub-channels produced using orthogonal frequency division multiplexing. To reduce the SNR required for a given bit error rate, the WiGLAN employs the use of multiple antennas to increase spatial diversity. Each antenna requires its own independent receiver. A description of the WiGLAN and some of the research ICs that were designed with this system driver will be presented.

A recent example of another system driver is an active mm-wave imaging system for automotive applications. Millimeter-wave radiation and detection offers the capability of two-dimensional imaging of

vehicles within the range of approximately 50-100 meters. Active transmission of a known signal modulated to carrier frequencies at 77 GHz and higher act as the "illumination" of the vehicle to be imaged. The reflected signal is scanned by an array of receivers (e.g. 32x32) to receive a number of "looks" at the object. After down-conversion to approximately 1 GHz, digitization of the signal is performed. Advanced digital signal processing is used to obtain intensity measurement of a two-dimensional array of "pixels" on the vehicle. It is expected that this system will guide mm-wave IC design for the next few years.

About the Speaker:



Charles G. Sodini currently is the LeBel Professor of Electrical Engineering at MIT. His research interests focus on mixed-signal integrated circuit and system design. He co-authored *Microelectronics: An Integrated Approach*, with Roger T. Howe, and is co-founder of SMA-L Camera Technologies, a leader in imaging technology for consumer digital still cameras and machine vision cameras for automotive applications. Prior to joining the MIT faculty in 1983, Sodini was a member of the technical staff at Hewlett-Packard Laboratories, working on MOS memory design. He is Chair of the Executive Committee for the VLSI Symposia and an IEEE Fellow.

Sodini was President of the IEEE Solid-State Circuits Society (2002-2004) and General Chairman of the International Electron Device Meeting (1989). In addition, he served on the IEEE Electron Device Society Administrative Committee. Sodini holds a B.S.E.E. degree from Purdue University, and M.S.E.E. and Ph.D. degrees from the University of California, Berkeley.

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**Keynote 3: Friday 25<sup>th</sup> Jan 2008,**  
**Lecture Theatre J, LTJ.**  
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13:20-14:00 Dr Stephen Lai, Solomon Systech, Hong Kong, "Technology Trend of Flat Panel Display Driver Electronics"

Abstract:

The technology trend of flat panel displays is amazingly diverse and accelerating in all aspects. Aside from the dominant LCD technology, there is a multitude of electronic display technologies that can easily exhaust the knowledge of even the most knowledgeable display experts. Plasma displays are still going strong in spite of the continual advance of the LCD. OLED is improving and is finding favorable applications. EPD's have been proven in many real product applications, definitely demonstrating great potentials without doubts. Display applications have penetrated into all areas of the consumer, computer, and communication markets.

For driver electronics to keep up with these amazing display technologies are no easy tasks. Driver electronics are indeed providing the driving forces for the commercialization of these display technologies, from enhancing the dominant technologies into ever increasing performance levels, to enabling the new emerging technologies or developing new applications. This talk will attempt to showcase the technology trend in this age of Display-Everywhere!

About the Speaker:



Dr. Stephen Wai-Yan Lai received the B.Sc. in electrical engineering from the University of Hong Kong in 1969, and the M.S.E.E. and Ph.D. in solid state engineering from the Syracuse University in 1971 and 1975, respectively.

Dr. Lai has been the Design Director of the Solomon Systech since its inception in 1999 and is responsible for system engineering, Integrated Circuit (IC) design and new technology.

He has 30 years of experience, majority from the U.S., in semiconductors and integrated circuits which include technology and product development and management, systems and circuits design and characterization, process and device research and development, design methodology and automation, and analytical instrumentation and semiconductors reliability. Prior to Solomon Systech, he was the Design Manager at the Display IC Division at Motorola Semiconductors Hong Kong Limited.

Tuesday 22nd Jan 2008

- 16:00** **REGISTRATION: UC Bistro,
Tower C, G/F, HKUST**
- 17:00** **Welcome Reception: UC Bistro,
Tower C, G/F, HKUST**

Wednesday 23rd Jan 2008

- 08:00** **REGISTRATION: Lecture Theatre
J, LTJ, HKUST**
- 09:00-09:10** **Opening Ceremony**
- 09:10-09:20** **Welcome Address: Professor
Roland Chin,
Vice President for Academic
Affairs, HKUST**
- 09:20-09:40** **Committees Address: General
and Program Chairs**
- 09:40-10:20** **Keynote by Professor Niraj K.
Jha, EE Department, Princeton
University, USA "Digital System
Testing: Emerging Issues, Trends
and Solution Approaches"
venue: Lecture Theatre J, LTJ.**

10:20-10:50 **BREAK**

10:50-12:10 **SESSION 1, (Lecture Theatres J and K, HKUST)**

10:50-12:10 **Session 1A: Analogue Design 1 Lecture Theatre J, LTJ.**

Chairs: Chung-Yu Wu (NCTU, Taiwan), Leung Lai Kan Lincoln (CUHK, Hong Kong)

- A Design of 14-bits ADC and DAC for CODEC Applications in 0.18 μ m CMOS process
Donghyun KO, Jihoon JUNG, younggun PU, SangKyung SUNG, KangYoon LEE, (Konkuk University, South Korea) Chul NAM (SiliconHarmony. South Korea)
- Compensation-Capacitor Free Pseudo Three-Stage Amplifier with Large Capacitive Loads
Ka NANG LEUNG, Yanqi ZHENG (The Chinese University of Hong Kong)
- The design and optimization of a 25kS/s 10bit Micropower Current S/H Cell for Weak Current Bio-medical Applications
Ka Leong TSANG, Jie YUAN (HKUST, Hong Kong)
- A Single-Stage SEPIC PFC Converter for Multiple Lighting LED Lamps
Hsiu-Ming HUANG, Shih-Hsiung TWU, Shih-Jen CHENG, Huang-Jen CHIU (National Taiwan University of Science and Technology)

10:50-12:10 **Session 1B: SoC and NoC Testing Lecture Theatre K, LTK.**

Chairs: Michel Renovell (LIRMM, France), Cheng-Wen Wu (NTHU, Taiwan)

- Using Genetic Evolutionary Software Application Testing to Verify a DSP SoC
Adriel CHENG, Cheng-Chew LIM (University of Adelaide, Australia) Yihe SUN, Hu HE, Zhixiong ZHOU, Ting LEI (Tsinghua University, China)

- Channel Width Utilization Improvement in Testing NoC-Based Systems for Test Time Reduction
Jia LI, Qiang XU, Yu HU, Xiaowei LI (ICT, Chinese Academy of Sciences, China)
- Coordinated versus Uncoordinated Checkpoint Recovery for Network-on-Chip based Systems
Claudia RUSU, Lorena ANGHEL (TIMA Laboratory, France)
Cristian GRECU (University of British Columbia, Canada)
- Testing of a Highly Reconfigurable Processor Core for Dependable Data Streaming Applications
Hans G. KERKHOFF (University of Twente, The Netherlands)
Jarkko J. M. HUIJTS (TDT, The Netherlands)

12:10-13:20 LUNCH at UC Bistro, Tower C, G/F, HKUST

13:20-15:00 SESSION 2 (Lecture Theatres J and K, HKUST)

13:20-15:00 Session 2A: Signal and Image Processing Lecture Theatre J, LTJ.

Chairs: Yuminosuke Yano (Ehime University, Japan), Kam Tim Woo (HKUST, Hong Kong)

- A Fast Algorithm for the Chirp Rate Estimation
Jihai CAO, Ning ZHANG, Lin SONG (Harbin Institute of Technology, China)
- Crack Detection on Asphalt Surface Image Using Enhanced Grid Cell Analysis
Siwaporn SORNCHAREAN, Suebskul PHIPHOBMONGKOL (Chulalongkorn University, Thailand)
- Image Model Use for 1D Near Optimal Interpolation for Image Super-resolution
Andrew GILMAN, Donald G. BAILEY, Stephen R. MARSLAND (Massey University, New Zealand)

- Performance Estimation of Crash Control System using Image Processing
Sriram MURALI, Ramachandran SHANKAR (Anna University, India)

13:20-15:00 Session 2B: Advanced Communication Systems Lecture Theatre K, LTK.

Chairs: Zhihua Wang (Tsinghua University, China), Farid Flitti (HKUST, Hong Kong)

- A High Speed CMOS Transmitter and Rail-to-Rail Receiver
Feng ZHANG, Lingyi HUANG, Weinwu HU (Institute of Computing Technology, China)
- Design of a 12-Channel 120-Gb/s Optical Receiver Array in 0.18- μm CMOS Technology
W. S. OH, K. PARK, J. C. CHOI, C. J. KIM, S. I. LEE, J. K. MOON (Korea Electronics Technology Institute, South Korea)
- 99-dB High-Performance Delta-Sigma Modulator for 20-kHz Bandwidth
Youngkil CHOI, Hyungdong ROH, Hyunseok NAM, Jeongjin ROH (Hanyang University, South Korea)
- Analysis and Design of a Continuous-Time Sigma-Delta Modulator with 20MHz Signal Bandwidth, 53.6dB Dynamic Range and 51.4dB SNDR
Tao WANG, Liping LIANG (Tsinghua University, China)

15:00-15:30 BREAK & POSTERS

15:00-15:30 Poster Session 1 Area outside Lecture Theatre K & J.

Chair: Abbes Amira (Brunel University, UK)

- An FPGA Implementation of the Searcher Algorithm
A. SAGAHYROON, M. EI TARHUNI, S. IBRAHIM (American University of Sharjah, United Arab Emirates)

- Analysis of CPU Utilisation and Stack Consumption of a Multimedia Embedded System
Amith KUMAR, Nuggehalli RAMACHANDRA, (Delphi Corporation, USA)
Avin Kumar KANNUR (Arizona State University, USA)
- Research on System Usability of Digital Libraries in China
Yaohua YU, Zhengjie LIU (Dalian Maritime University, China)
- A Fast Two-Stage Sample-and-Hold Amplifier for Pipelined ADC Application
Jian RUAN, (Peking University, China)
Chung Len LEE (National Chiao Tung University, Taiwan)
- Low Phase Noise Bond Wire VCO for DVB-H
Ki-Jin KIM, K. H. AHN, T. H. LIM (Korea Electronics Technology Institute, South Korea)
- A Novel Dummy bitline Driver for Read Margin Improvement in an eSRAM
M. Yap San MIN, P. MAURINE, M. BASTIAN, M. ROBERT (LIRMM, France)
- A 14-bit 320MSPS Segmented Current-steering D/A Converter for High-speed Application
Shangquan LIANG, Minglun GAO, Yongsheng YIN, Honghui DENG (Hefei University of Technology, China)
- A Multiprocessor System for a Small Size Soccer Robot Control System
Ce LI, Yang JIANG, Zhenyu WU, Takahiro WATANABE (Waseda University, Japan)
- Low Cost Arbitration Method for Arbitrarily Scalable Multiprocessor Systems
Tero VALLIUS, Juha RÖNING (University of Oulu, Finland)
- An Efficient Design of Single Event Transients Tolerance for Logic Circuits
Yantu MO, Suge YUE (Beijing Microelectronic Technology Institute, China)

- Adaptive Diagnostic Pattern Generation for Scan Chain
Fei WANG, Yu HU, Xiaowei LI (ICT, Chinese Academy of Sciences, China)
- Built-In Self-Test for Embedded Voltage Regulator
Jiang SHI, Ricky SMITH (Texas Instruments, USA)

15:30-17:10 SESSION 3 (Lecture Theatres J and K, HKUST)

15:30-17:10 Session 3A: Special Session on High Performance Reconfigurable Computing / Lecture Theatre J, LTJ.

Chairs: Abbes Amira (Brunel University, UK), Oliver Pfaender (Ulm University, Germany)

- Recent Trends in FPGA Architectures and Applications (invited talk)
Philip H. W. LEONG (Chinese University of Hong Kong)
- Embedding Smart Buffers for Window Operations in a Stream-Oriented C-to-VHDL Compiler
Fabian DIET, Erik H. D'HOLLANDER, Kristof BEYLS, Harald DEVOS (Ghent University, Belgium)
- Implementation of Hardware Encryption Engine for Wireless Communication on a Reconfigurable Instruction Cell Architecture
Zong WANG, Tughrul ARSLAN, Ahmet ERDOGAN (University of Edinburgh, UK)
- Dynamic slowdown and partial reconfiguration to enhance power and scalability in FPGA based auto-adaptive SoPC
Xun ZHANG, Hassan RABAH, Serge WEBER (Nancy Université, France)
- xDSL Network Upgrade Employing FPGAs
Milos MILOSAVLJEVIC, Faycal BENSALI, Pandelis KOURTESSIS (University of Hertfordshire, UK)

**15:30-17:10 Session 3B: Sensor, Implants and Display
Lecture Theatre K, LTK.**

Chairs: Hong Chen (Tsinghua University, China), Farid Boussaid (UWA, Australia)

- Architecture of a Low Storage Digital Pixel Sensor Array with an On-line Block-Based Compression
Milin ZHANG, Amine BERMAK (HKUST, Hong Kong)
- Effects of insulator thickness on the sensing properties of MISiC Schottky-diode hydrogen sensor
W. M. TANG, C. H. LEUNG, P. T. LAI (HKU, Hong Kong)
- High Speed Depth Estimation using Tilted Focal Planes
Hiroshi IKEOKA, Takayuki HAMAMOTO (Tokyo University of Science, Japan)
- Multi-Phase Charge Pump Generating Positive and Negative High Voltages for TFT-LCD Gate Driving
Chi-Hao WU, Chern-Lin CHEN (National Taiwan University, Taiwan)
- Power Issues on Circuit Design for Cochlear Implants (invited talk)
Zhihua WANG, Songping MAI, Chun ZHANG (Tsinghua University, China)

Thursday 24th Jan 2008

08:40-10:00 SESSION 4 (Lecture Theatres J and K, HKUST)

**08:40-10:00 Session 4A: Advanced Memory Design
Lecture Theatre J, LTJ.**

Chairs: Zhang Feng (ICT, China), Kong Pang Pun (CUHK, Hong Kong)

- Dynamic Co-operative Intelligent Memory
Xiaoyong WEN, Faycal BENSALI, Reza SOTUDEH (University of Hertfordshire, UK)

- An Accurate and Energy-Efficient Way Determination Technique for Instruction Caches by Using Early Tag Matching
*Eui-Young CHUNG, (Yonsei University, South Korea)
Cheol Hong KIM, (Chonnam National University, South Korea)
Sung Woo CHUNG (Korea University, South Korea)*
- Proposal for a Bidirectional Gate using Pseudo Floating-Gate
O. MIRMOTAHARI, Y. BERG (University of Oslo, Norway)
- Read Stability and Write Ability Trade-off for 6T SRAM Cells in Double-Gate CMOS
Bastien GIRAUD, Amara AMARA (ISEP, France)

**08:40-10:00 Session 4B: Signal, Faults and Yield
modelling / Lecture Theatre K, LTK.**

Chairs: Marcel Jacomet (Bern University of Applied Science, Switzerland), Xiaowei Li (ICT, China)

- Compact Models for Signal Transient and Crosstalk Noise of Coupled RLC Interconnect Lines with Ramp Inputs
Taehoon KIM, Dongchul KIM, Jung-A LEE, Yungseon EO (Hanyang University, South Korea)
- Improving Diagnosis Resolution without Physical Information
A. ROUSSET, A. BOSIO, P. GIRARD, C. LANDRAULT, S. PRAVOSSOUDOVITCH, A. VIRAZEL (LIRMM, France)
- Predictive Die-Level Reliability-Yield Modelling
*Melanie Po-Leen OOI, Ye Chow KUANG, (Monash University Sunway Campus, Malaysia)
Chris CHAN, (Freescale Semiconductor, Malaysia) Serge DEMIDENKO (Massey University, New Zealand)*
- Hierarchical Calculation of Malicious Faults for Evaluating the Fault-Tolerance
Raimund UBAR, Sergei DEVADZE, Maksim JENIHHIN, Jaan RAIK, Gert JERVAN, Peeter ELLERVEE (Tallinn Technical University, Estonia)

10:00-10:30 BREAK & POSTERS

10:00-10:30 Poster Session 2 Area outside Lecture Theatre K & J.

Chair: Abbas Amira (Brunel University, UK)

- FPGA implementation of a Single Pass Connected Components Algorithm
Christopher T. JOHNSTON, Donald G. BAILEY (Massey University, New Zealand)
- A low voltage rail-to-rail OPAMP design for biomedical signal filtering applications
Hwang-Cherng CHOW, Pu-Nan WENG
- Workload-Based Dynamic Voltage Scaling with the QoS for Streaming Video
Hong Moon WANG, Hyun Suk CHOI, Jong Tae KIM (Sungkyunkwan University, South Korea)
- Speech Recognition of Isolated Malayalam Words Using Wavelet Features and Artificial Neural Network
Vimal V. R. KRISHNAN, Athulya JAYAKUMAR, P. Babu ANTO (Kannur University, India)
- FPGA based Real Time Solution for Sensitivity Time Control
D. MEENA, L. G. M. PRAKASAM (Electronics and Radar Development Establishment, India)
- A Jittered-Sampling Correction Technique for ADCs
Jamiil TOURABALY, Adam OSSEIRAN (ECU, Australia)
- Robust JPEG2000 Image Transmission over IEEE 802.15.4
Kyu-Yeul WANG, Seung-Yerl LEE, Byung-Soo KIM, Sang-Seol LEE, Jae-Yeon SONG, Duck-Jin CHUNG (Inha University, South Korea), Dong-Sun KIM (Korea Electronics Technology Institute, South Korea)
- New D-Type Flip-Flop Design Using Negative Differential
Dong-Shong LIANG, Kwang-Jow GAN (Kun Shan University, Taiwan)

- Experimental Characterisations of Coupled Transmission Lines
Dongchul KIM, Taehoon KIM, Jung-A LEE, Yungseon EO (Hanyang University, South Korea)
- A Low Power Deterministic Test Pattern Generator for BIST Based on Cellular Automata
Bei CAO, Liyi XIAO, Yongsheng WANG (Harbin Institute of Technology, China)
- A Test Data Compression Method for System-on-a-Chip
Jianhua FENG, Guoliang LI (Peking University, China)

10:30-12:10 SESSION 5 (Lecture Theatres J and K, HKUST)

10:30-12:10 Session 5A: DSP and Processor Design Lecture Theatre J, LTJ.

Chairs: Donald Bailey (Massey University, New Zealand), Oliver Pfaender (Ulm University, Germany)

- A hybrid of clonal selection algorithm and frequency sampling method for designing a 2-D FIR filter
Te-Jen SU, Chun-Hsiang KUO, Wen-Pin TSAI, Cheng-Chih HOU (National Kaohsiung University of Applied Sciences, Taiwan)
- A Generation Flow for Self-Reconfiguration Controllers Customization
Andrea CUOCCIO, Paolo R. GRASSI, Vincenzo RANA, Marco D. SANTAMBROGIO, Donatella SCIUTO (Politecnico di Milano, Italy)
- Design of High-Speed Floating Point Multiplier
Saroja V. SIDDAMAL, R. M. BANAKAR (BVBCET, India), B. C. JINAGA (JNTU, India)
- High Performance Elliptic Curve Cryptographic Processor Over GF(2¹⁶³)
Hyun Min CHOI, Chun Pyo HONG, Chang Hoon KIM (Daegu University, South Korea)

- A Visual Notation for Processor and Resource Scheduling
Christopher T. JOHNSTON, Paul LYONS, Donald G. BAILEY (Massey University, New Zealand)

10:30-12:10 Session 5B: DfT and BIST Lecture Theatre K, LTK.

Chairs: Hans Kerkhoff (University of Twente, The Netherlands),
Hiromi Hiraishi (Kyoto Sangyo University, Japan)

- Design For Testability of Functional Cores for High Performance Node Architectures
Venkateswaran NAGARAJAN, Karthik CHANDRASEKAR, Shrikanth GANAPATHY (Waran Research Foundation, India)
- Test Response Data Volume and Wire Length Reductions for Extended Compatibilities Scan Tree Construction
Yong-sheng CHENG, Zhi-qiang YOU, Ji-shun KUANG (Hunan University, China)
- AES-based BIST: self-test, test pattern generation and signature analysis
M. DOULCIER, M.-L. FLOTTES, B. ROUZEYRE (LIRMM, France)
- Oscillation-Based Test in Data Converters: On-line Monitoring
Gloria HUERTAS (IMSE-CNM, Spain)
Jose L. HUERTAS (Universidad De Sevilla, Spain)
- A case study on At-Speed Testing of a Gigahertz Microprocessor
Da WANG, Rui LI, Yu HU, Huawei LI, Xiaowei LI (ICT, Chinese Academy of Sciences, China)

12:10-13:20 LUNCH; Chinese Restaurant, G/F, HKUST

13:20-14:40 SESSION 6 (Lecture Theatres J and K, HKUST)

13:20-14:40 Session 6A: Analogue Design 2 Lecture Theatre J, LTJ.

Chairs: Alex Ka Nang Leung (CUHK, Hong Kong), Adam Osseiran (ECU, Australia)

- A charge pump circuit -- cascading high-voltage clock generator
Wen Chang HUANG, Po Chih LIOU (Kun Shan University, Taiwan)
Jin Chang CHENG (Chang Jung Christian University, Taiwan)
- Threshold Voltage Start-up Boost Converter for Sub-mA Applications
Ngok-Man SZE, Wing-Hung KI, Chi-Ying TSUI (HKUST, Hong Kong)
- Design of a Low-Voltage CMOS Charge Pump
Chun Yu CHENG, Ka Nang LEUNG, Yi Ki SUN, Pui Ying OR (The Chinese University of Hong Kong)
- High-Input Impedance Voltage-Mode Universal Biquadratic Filter with One input and Five Outputs using DDCCs
Wei-Yuan CHIU, Jiun-Wei HORNG, Shyuan-Shenq YANG (Chung Yuan Christian University, Taiwan)

13:20-14:40 Session 6B: Energy and Cost Efficient Reconfigurable Systems / Lecture Theatre K, LTK.

Chairs: Hans-Joerg Pflaederer (Ulm University, Germany), Philip Leong (CUHK, Hong Kong)

- Temporal-Spatial Correlation Based Mode Decision Algorithm for H.264/AVC Encoder
Bin ZHAN, Baochun HOU, Reza SOTUDEH (University of Hertfordshire, UK)
- A Software-to-Hardware Self-Mapping Technique to Enhance Program Throughput for Portable Multimedia Workloads
Allen C. CHENG (University of Pittsburgh, USA)
- Improved Policies for Drowsy Caches in Embedded Processors
Junpei ZUSHI, Gang ZENG, Hiroyuki TOMIYAMA, Hiroaki TAKADA (Nagoya University, Japan)
Koji INOUE (Kyushu University, Japan)

- Improving cost-effectiveness using a micro-level static architecture for stream applications
Pil Woo CHUN, Jamin ISLAM, Valeri KIRISCHIAN, Lev KIRISCHIAN (Ryerson University, Canada)

14:40-15:20 BREAK & POSTERS

14:40-15:20 Poster Session 3: Special Session on Advanced Biometric and Security Systems / Area outside Lecture Theatre K & J.

Chair: Abbas Amira (Brunel University, UK)

- A compact CMOS Face Detection architecture based on Shunting Inhibitory Convolutional Neural Networks
Xiaoxiao ZHANG, Amine BERMAK (HKUST, Hong Kong)
Farid BOUSSAID (UWA, Australia)
Abdesselam BOUZERDOUM (Wollongong University, Australia)
- Temperature Modulation for Tin-Oxide Gas Sensors
Aicha FAR, Bin GUO, Farid FLITTI, Amine BERMAK (HKUST, Hong Kong)
- Eigenspectra Palmprint Recognition
Moussadek LAADJEL, Ahmed BOURIDANE, Fatih KURUGOLLU (Queens University, UK)
- VLSI architecture and FPGA implementation of a hybrid message embedded self-synchronizing stream cipher
Camel Tanougast, S. WEBER, Gilles MILLERIOUX, J. DAAFOUZ (University Henri Poincaré, France)
Ahmed BOURIDANE (Queens University, UK)
- DWT/PCA Face Recognition using Automatic Coefficient Selection
Paul NICHOLL (Queens University, UK)
Abbas AMIRA (Brunel University, UK)
- A Spiking Neural Network for Gas Discrimination using a Tin Oxide Sensor Array
Maxime AMBARD, Dominique MARTINEZ (LORIA-INRIA, France)
Bin GUO, Amine BERMAK (HKUST, Hong Kong)

15:20-16:00 Keynote by Professor Charles Sodini, Massachusetts Institute of Technology, USA, "System Drivers for Mixed Signal Integrated Circuit Design Research"
venue: Lecture Theatre J, LTJ.

17:30-22:00 SOCIAL EVENT & BANQUET: "BOAT CRUISE"

Friday 25th Jan 2008

09:00-10:20 SESSION 7 (Lecture Theatres J and K, HKUST)

09:00-10:20 Session 7A: NoC and SoC Design Lecture Theatre J, LTJ.

Chairs: Stefan Lachowicz (ECU, Australia), Gourab Sen Gupta (Massey University, New Zealand)

- A Hybrid Interconnect Network-on-Chip and a Transaction Level Modeling approach for Reconfigurable Computing
Thomas LENART, Henrik SVENSSON, Viktor ÖWALL (Lund University, Sweden)
- A Requirements-Driven Reconfigurable SoC Communication Infrastructure Design Flow
Alessandro MERONI, Vincenzo RANA, Marco SANTAMBROGIO, Donatella SCIUTO (Politecnico di Milano, Italy)
- High-Speed Priority Queue Architecture for Multiple Out-Links
Sang Gyun KIM, Woo Sik KIM, Seung Ho OK, Byung In MOON (Kyungpook National University, South Korea)

- Integrated Mapping and Scheduling for Circuit-Switched Network-on-Chip Architectures
Hsin-Chou CHI, Chia-Ming WU, Jun-Hui LEE (National Dong Hwa University, Taiwan)

09:00-10:20 Session 7B: Systems and Sensors Lecture Theatre K, LTK.

Chairs: Jie George Yuan (HKUST, Hong Kong), Achim Rettberg (Universitaet Paderborn, Germany)

- Drift invariant Gas Recognition Technique For Tin Oxide Gas Sensor array
Farid FLITTI, Aicha FAR, Bin GUO, Amine BERMAK (HKUST, Hong Kong)
- On Using Fingerprint-Sensors for PIN-Pad Entry
*Marcel JACOMET, Josef GOETTE (Bern University of Applied Sciences, Switzerland)
Andreas EICHER (AXSionics Inc., Switzerland)*
- FPGA Implementation of a Predictive Vector Quantization image compression algorithm for image sensor applications
*Yan WANG, Amine BERMAK (HKUST, Hong Kong)
Abdesselam BOUZERDOUM (Wollongong University, Australia)
Brian NG (University of Adelaide, Australia)*
- Integrating Dynamic Load Balancing Strategies into the Car-Network
Isabell JAHNICH, Ina PODOLSKI, Achim RETTBERG (Universitaet Paderborn, Germany)

10:20-10:50 BREAK & POSTERS

10:20-10:50 Poster Session 4 Area outside Lecture Theatre K & J.

Chair: Abbes Amira (Brunel University, UK)

- A Design of the Frequency Synthesizer for UWB Application in 0.13 μm RF CMOS process
*JinKyung KIM, Sung-Kyu JUNG, Ji-Hoon JUNG, Sang-Kyung SUNG, Kang-Yoon LEE (KonKuk University, South Korea)
Chul NAM (SiliconHarmony, South Korea)
Bong-Hyuk PARK, Sang-sung CHOI (ETRI, South Korea)*
- Analog to Digital Converter Specifications for UMTS/FDD Receiver Application
Zulhakimi RAZAK, Tughrul ARSLAN (University of Edinburgh, UK)
- A Design Workflow for the Identification of Area Constraints in Dynamic Reconfigurable Systems
Alessio MONTONE, Marco D. SANTAMBROGIO, Donatella SCIUTO (Politecnico di Milano, Italy)
- Bus Binding, Re-ordering, and Encoding for Crosstalk-producing Switching Activity Minimization during High Level Synthesis
Hariharan SANKARAN, Srinivas KATKOORI (University of South Florida, USA)
- Scalable Montgomery Multiplier for Finite Fields GF(p) and GF(2^m)
Tae Ho KIM, Sang Chul KIM, Chang Hoon KIM, Chun Pyo HONG (Daegu University, South Korea)
- Static Crosstalk Noise Analysis with Transition Map
Minjin ZHANG, Huawei LI, Xiaowei LI (ICT, Chinese Academy of Sciences, China)
- Implementation of the Embedded System for Visually-Impaired People
Si-Woo KIM, Jae-Kyun LEE, Boo-Shik RYU, Chae-Wook LEE (Daegu University, South Korea)
- Model-based Gaze Direction Estimation in Office Environment
Do Joon JUNG, Kyung Su KWON, Se Hyun PARK, Jong Bae KIM, Hang Joon KIM (Daegu University, South Korea)

- Fast Evaluation of the Square Root and Other Nonlinear Functions in FPGA
Stefan LACHOWICZ (ECU, Australia)
Hans-Jörg PFLEIDERER (Ulm University, Germany)
- Configurable Blocks for Multi-Precision Multiplication
Oliver A. PFÄNDER, Reinhard NOPPER, Hans-Jörg PFLEIDERER (Ulm University, Germany)
Shun ZHOU, Amine BERMAK (HKUST, Hong Kong)
- High Performance FPGA Implementation of the Mersenne Twister
Shrutisagar CHANDRASEKARAN, Abbas AMIRA (Brunel University, UK)
- Static Crosstalk Noise Analysis with Transition Map
A. BOUHRAOUA, M. E. ELRABAA (KFUPM, Saudi Arabia)

10:50-12:10 SESSION 8 (Lecture Theatres J and K, HKUST)

10:50-12:10 Session 8A: Special Session on Smart Sensors Lecture Theatre J, LTJ.

Chairs: Amara Amara (ISEP, France), Subhas Mukhopadhyay (Massey University, New Zealand)

- The Fourier Spectrum Analysis of Optical Feedback Self-Mixing Signal under Weak and Moderate Feedback
Xiaojun ZHANG, Jiangtao XI, Yanguang YU, Joe CHICHARO (University Wollongong, Australia)
- Elimination of Non-linear Luminance Effects for Digital Video Projection Phase Measuring Profilometers
Matthew BAKER, Jiangtao XI, Joe CHICHARO (University Wollongong, Australia)
- Integrated CMOS analog neural network ability to linearise the distorted characteristic of HPA embedded in satellites
Laurent GATET, Francis GIZARD (CNES, France)
Hélène TAP-BETEILLE, Daniel ROVIRAS (ENSEEIH, France)

- Compact Gray-Code Counter/Memory Circuits for Spiking Pixels
Kwan Ting NG, Farid BOUSSAID (UWA, Australia)
Chen SHOUSHUN, Amine BERMAK (HKUST, Hong Kong)

10:50-12:10 Session 8B: Advanced Testing Techniques Lecture Theatre K, LTK.

Chairs: JoseLuis Huertas (Universidad De Sevilla, Spain)
Shiyi Xu (Shanghai Uni. of S&T, China)

- Calibration and Debugging of Multi-Step Analog to Digital Converters
Amir ZJAJO, Jose PINEDA de GYVEZ (NXP Semiconductors Research, The Netherlands)
- A Convenient Voltage Stress Test Method for High Density Memory
Jongsoo YIM, Gunbae KIM, Sungho KANG (Yonsei University, South Korea)
Incheol NAM, Sangki SON, Jonghyoung LIM, Hwacheol LEE, Sangseok KANG, Byungheon KWAK, Jinseok LEE (Samsung Electronics, South Korea)
- A Scan-based delay test method for reduction of overtesting
Hui LIU, Huawei LI, Yu HU, Xiaowei LI (ICT, Chinese Academy of Sciences, China)
- An Integrated Validation Environment for Differential Power Analysis
Giorgio Di NATALE, Marie-Lise FLOTTES, Bruno ROUZEYRE (LIRMM, France)
- Automated Testing of FlexRay Clusters for System Inconsistencies in Automotive Networks
Paul MILBREDT (AUDI AG, Germany)
Andreas STEININGER (Technische Universität Wien, Austria)
Martin HORAUER (University of Applied Sciences Technikum Vienna, Austria)

12:10-13:20 LUNCH, Chinese Restaurant, G/F, HKUST

**13:20-14:00 Keynote by Dr Stephen Lai,
Solomon Systech, HK**
"Technology Trend of Flat Panel
Display Driver Electronics"
venue: Lecture Theatre J, LTJ.

**14:00-15:20 SESSION 9 (Lecture Theatres J
and K, HKUST)**

**14:00-15:20 Session 9A: Power Issues in Design
Lecture Theatre J, LTJ.**

Chairs: Zhihua Wang (Tsinghua University, China), Patrick Girard (LIRMM, France)

- Early Design Phase Power Performance Trade-offs Using In-situ Macro Models
Charles THANGARAJ, Tom CHEN (Colorado State University, USA)
- Low Voltage Design against Power Analysis Attacks
O. MIRMOTAHARI, Y. BERG (University of Oslo, Norway)
- Electrical Power Monitoring System using ThermoChron Sensor and 1-Wire Communication Protocol
Moi-Tin CHEW (Massey University, New Zealand)
Tatt-Huong THAM, Ye-Chow KUANG (Monash University Malaysia Campus, Malaysia)
- Infrastructure for Microelectronics Education, Research and SMEs (*Special Presentation*)
Bernard COURTOIS (CMP, France)

**14:00-15:20 Session 9B: VLSI System Design
Lecture Theatre K, LTK.**

Chairs: Ton Mouthaan (Twente University, the Netherlands), Igor Lemberski (BIA, Latvia)

- Efficient VLSI layout of Edge Product Networks
Saeedeh BAKHSHI, Hamid SARBAZI-AZAD (Sharif University of Technology, Iran)
- Towards a Petri Net based Approach to Model and Synthesize Dynamic Reconfiguration for FPGAs
Helene SCHILKE, Achim RETTBERG, Florian DITTMANN (Universitaet Paderborn, Germany)
- Arbitrary Waveform Generator Based on Direct Digital Frequency Synthesizer
Weibo HU, Xin'an WANG (Peking University, China)
Chung Len LEE (National Chiao Tung University, Taiwan)
- Design of a Data Concentrator Card for the Readout of the Compact Muon Solenoid Electromagnetic Calorimeter
Jose Carlos Da SILVA, Michal HUJESKO (LIP-Lisbon, Portugal)
Joao VARELA (CERN, Switzerland)

15:20-15:40 BREAK

**15:40-16:40 SESSION 10 (Lecture Theatres J
and K, HKUST)**

**15:40-16:40 Session 10A: Advanced and high-level test
methods / Lecture Theatre J, LTJ.**

Chairs: Bernard Courtois (CMP, France), Bruno Rouzeyre (LIRMM, France)

- A Novel Approach to High-level Property Checking Using Wu's Method
Zhi YANG, Guangsheng MA, Shu ZHANG (Harbin Engineering University, China)
- Test Set Stripping Limiting the Maximum Number of Specified Bits
Michael A. KOCHTE, Christian G. ZOELLIN, Michael E. IMHOF, Hans-Joachim WUNDERLICH (Universitaet Stuttgart, Germany)

- An Automated Fault Injection Technique Based on VHDL Syntax Analysis and Stratified Sampling
Weiguang SHENG, Liyi XIAO, Zhigang MAO (Harbin Institute of Technology, China)

15:40-16:40 Session 10B: Advanced Applications
Lecture Theatre K, LTK.

Chairs: Serge Demidenko, Moi-Tin Chew (Massey University, New Zealand)

- CreaTe: A new programme to attract engineers as design artists
Zsofi RUTTKAY, Ton MOUTHAN (University of Twente, The Netherlands)
- High-Performance Pseudorandom Number Generator Using Two-Dimensional Cellular Automata
Byung-Heon KAN, Dong-Ho LEE, Chun-Pyo HONG (Daegu University, South Korea)
- Design Automation of UHF RFID Tag Antenna Using a Genetic Algorithm Linked with MWS CST
Kyounghwan LEE, Youngju KIM, Goojo KIM, You Chung CHUNG (Daegu University, South Korea)

16:40-17:00 CLOSING SESSION –Closing remarks by the conference chairs, Best paper awards

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Delta 2008 - Transportation:

| Date | Conference time | From hotels to HKUST | From HKUST |
|---------------------------------|-----------------|--|--|
| 23 Jan. 2008 (Wed.) | 9:00 → 17:10 | <ul style="list-style-type: none"> • Pickup at TST⁰ • 8:00 – Marco Polo HK Hotel • 8:10 – Kowloon Hotel • Drop-off at HKUST | <ul style="list-style-type: none"> • 17:40 - Pickup at HKUST • Drop-off at Marco Polo HK Hotel and then Kowloon Hotel |
| 24 Jan. 2008 (Thur.) | 8:40 → 16:00 | <ul style="list-style-type: none"> • Pickup at TST • 7:40 – Marco Polo HK Hotel • 7:50 – Kowloon Hotel • Drop-off at HKUST | <ul style="list-style-type: none"> • 17:20 – Pickup at HKUST • Drop-off at North Point Ferry Pier (Banquet) (Around 120 guests; Two shuttle buses) |
| 25 Jan. 2008 (Fri.) | 9:00 → 17:00 | <ul style="list-style-type: none"> • Pickup at TST • 8:00 – Marco Polo HK Hotel • 8:10 – Kowloon Hotel • Drop-off at HKUST | <ul style="list-style-type: none"> • 17:30 - Pickup at HKUST • Drop-off at Marco Polo HK Hotel and then Kowloon Hotel |

(*) Tsim Sha Tsui

Public Transportation:

Public transportation in Hong Kong is very efficient, and getting to and from HKUST by taxi, the MTR metro, or bus is easy, as is accessibility by car.

The main gate of the campus features a large and easily recognizable sign with the university's name written in both English and Chinese. Past the main gate, a gently sloping driveway leads to the entrance piazza with a large red sundial at its center.

MTR

The Mass Transit Railway (MTR) is an underground subway (metro) system serving Hong Kong island, Kowloon, and the airport. The MTR is the easiest way for visitors to get around Hong Kong. Tickets can be purchased from machines in the stations on a trip-by-trip basis or you can purchase multi-use Octopus cards at MTR ticket windows.

The Choi Hung, Lam Tin and Hang Hau MTR stations are the closest to the University, and you can board a bus or taxi (details below) to the main entrance of HKUST.

Taxi

Taxis provide the simplest way to get to the University, and are easily available at any MTR station, from hotels and most areas of Hong Kong. From the airport, you can take a taxi at the airport taxi stand and expect to pay approximately HK\$380 (about US\$49) for the journey. Note that only HK dollars will be accepted by your driver.

Print a copy of this page and the map and bring it with you in case you need to show the route or University name and address in Chinese to the taxi driver. The taxi drop-off point on campus is near the red sundial. For on-campus housing destinations, ask

the security guard at the main gate to give the taxi driver directions.

Buses/Minibuses

| | |
|---------------------------------|----------------------|
| From Choi Hung MTR station: | 11S minibus |
| From Hang Hau MTR station: | 11M minibus |
| From Diamond Hill MTR station: | 91, 91M buses |
| From Po Lam MTR station: | 91M bus, 12 minibus |
| From Ngau Tau Kok MTR station: | 104 minibus |
| From Tiu Keng Leng MTR station: | 792M |
| From Sai Kung: | 792M bus, 12 minibus |

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From Hong Kong Island: Take the Eastern Harbour Crossing towards Lam Tin. Continue straight after the roundabout, and get in the right lane towards the Tseung Kwan O Tunnel, following signs for Hang Hau. At the roundabout for Hang Hau, take the Ying Yip Road exit, following the road past the Clearwater Bay Film Studio onto Clearwater Bay Road, and follow signs for HKUST.

From Kowloon: Take Prince Edward Road towards Kwun Tong; after Choi Hung Estates, stay left and follow signs to Clearwater Bay. Take Clearwater Bay road and follow signs to HKUST.

From Shatin: Take Cairns or Lion Rock Tunnel, staying left onto Lung Cheung Road. Follow signs to Sai Kung. Take Clearwater Bay road, following signs for HKUST.

Map of the Conference Site

