PWM Digital Pixel Sensor Based on Asynchronous Self-Resetting Scheme

Alistair Kitchen, Amine Bermak, *Senior Member, IEEE*, and Abdesselam Bouzerdoum, *Senior Member, IEEE*

***Abstract*—In this letter, a pulse-width modulated digital pixel sensor is presented along with its inherent advantages such as low power consumption and wide operating range. The pixel, which comprises an analog processor and an 8-bit memory cell, operates in an asynchronous self-resetting mode. In contrast to most CMOS image sensors, in our approach, the photocurrent signal is encoded as a pulse-width signal, and converted to an 8-bit digital code using a Gray counter. The dynamic range of the pixel can be adapted by simply modulating the clock frequency of the counter. To test the operation of the proposed pixel architecture, an image sensor array has been designed and fabricated in a 0.35-μm CMOS technology, where each pixel occupies an area of 45 × 45 μm^2. Here, the operation of the sensor is demonstrated through experimental results.**

***Index Terms*—Asynchronous self-reset, CMOS imagers, pulse-width modulated (PWM) pixel, vision sensor.**

I. INTRODUCTION

THE CONTINUING advancement of deep submicrometer CMOS technologies has played a key role in introducing new concepts in the field of image sensors. After the passive pixel sensor (PPS), which only includes a photodetector and a select transistor, the active pixel sensor (APS) was introduced and today, the digital pixel sensor (DPS) is commonly employed in order to achieve on-pixel analogue-to-digital conversion [1]. However, a number of issues still need to be resolved in order to enable CMOS image sensors to continue taking advantage of the aggressive level of integration found in deep submicrometer technologies. Key issues that need particular attention include power consumption and dynamic range. The latter is constantly being reduced in deep submicrometer technology due to the continuing aggressive reduction of the supply voltage. The limited dynamic range imposed in deep submicrometer technologies is even worse for vision sensors applications as natural light levels can vary by over eight orders of magnitude and the limited voltage swing would make it impossible to represent such wide illumination ranges. To increase the dynamic range multiple-sampling [2] as well as synchronous self-resetting architectures or pulse frequency modulation (PFM) schemes have been proposed [3]–[5]. However, multiple capture techniques result in increased complexity, as well as higher power consumption and slower operation, as multiple frames are combined in order to obtain a single frame. The synchronous self-resetting scheme improves the dynamic range by recycling the well such that higher photocurrents are detected. Unfortunately, the synchronous self-resetting scheme suffers from higher dynamic power consumption as the pixel is constantly allowed to fire whenever it reaches a threshold voltage. In addition, DPS is very inefficiently realized using the synchronous self-resetting scheme, as an area-consuming digital counter is required at the pixel level [3].

In this letter, a new DPS based on a low-power asynchronous self-resetting scheme is designed, fabricated using 0.35 μm technology, and successfully tested. Although the pixel self-resets in a manner similar to some PFM pixels [5], [6], it is fundamentally different from free-running PFM pixels, as it is based on a PWM scheme as well as a new asynchronous self-resetting approach. The latter uses a start integration signal instead of a global reset signal, thereby avoiding the large peak currents encountered in a synchronous reset. The pixel also incorporates an on-pixel memory allowing the captured data to be randomly, and repeatedly, accessed. In addition, a programmable dynamic range is obtained through simple modulation of the digital clock signal of the timing circuit. A description of the pixel architecture is given in Section II. Experimental results are presented in Section III, followed by a conclusion in Section IV.

II. PIXEL ARCHITECTURE

The architecture of the DPS based on asynchronous self-resetting scheme is shown in Fig. 1(a). Each pixel is composed of a photosensitive device (reverse-biased photodiode P_d), a reset transistor $M1$, a comparator, an SR latch, and an 8-bit on pixel memory. During the reset operation, the voltage at the sensing node of the photodiode (V_N) is reset to V_c. The conversion process is started by triggering the St_{int} signal, which disconnects the photodiode from its reset path [Fig. 1(b)]. The light falling onto the photodiode discharges the internal capacitor of the photodiode C_d, resulting in a decreased voltage V_N across the photodiode node, as shown in Fig. 1(b). Once the voltage V_N reaches a reference voltage, V_{ref}, the output of the comparator (V_{out}) switches. The pulse obtained from the start of integration to the switching time of the comparator corresponds to the discharge time of the photodiode and can be described as a pulse width modulated (PWM) signal. The relationship between the discharge time (or pulse width) T_d and the photocurrent I_d is given by

$$T_d = \frac{(V_{\text{c}} - V_{\text{ref}}) \times C_d}{I_d}. \tag{1}$$

Manuscript received April 26, 2004; revised May 6, 2004. This work was supported in part by the Australian Research Council. The review of this letter was arranged by Editor P. Yu.

A. Kitchen and A. Bouzerdoum are with the School of Engineering and Mathematics, Edith Cowan University, Joondalup WA 6027, Australia (e-mail: a.kitchen@ecu.edu.au; a.bouzerdoum@ecu.edu.au).

A. Bermak is with Electronics and Electrical Engineering Department, Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: bermak@ieee.org).

Digital Object Identifier 10.1109/LED.2004.831222

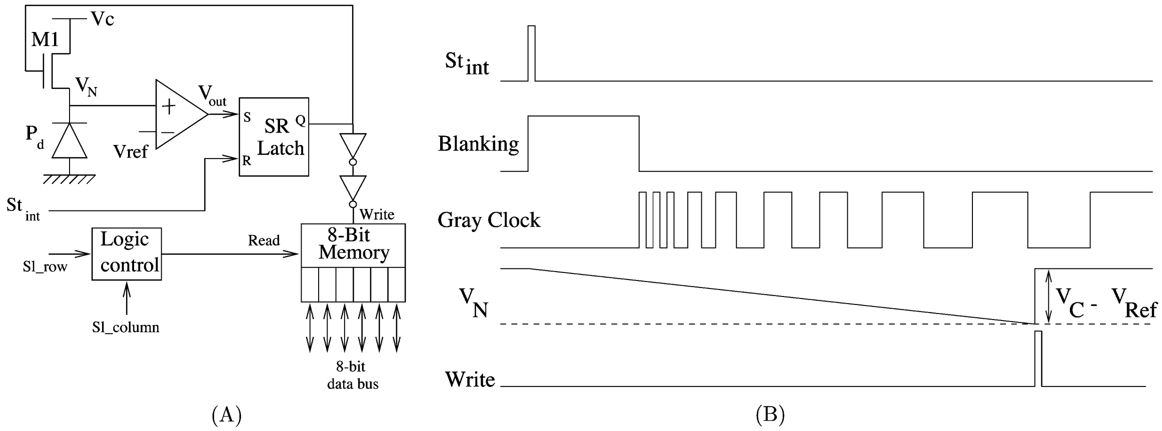

Fig. 1. (a) Digital pixel block diagram. (b) Timing diagram.

Unlike conventional vision sensors, a start integration signal St_{int} is used instead of a global reset signal, avoiding large peak current during the reset phase. The SR latch is used to obtain the asynchronous self-resetting operation. The pulse generated from the comparator is used to set the SR latch, which resets the photodiode voltage to V_c, and maintains it until a new start integration signal (St_{int}) is received. The pulse generated from the comparator, representing an asynchronous self-reset signal, is also used as a write signal allowing the data to be loaded into the on-pixel memory, using a global 8-bit Gray data bus. The local memories are therefore loaded in an asynchronous way when the comparator switches (end of the pulse width). In order to set the upper limit of the conversion process, the clock signal must be suppressed or "blanked" for a period of time for which the blanking signal is high as shown in Fig. 1(b). It is only after the end of the blanking period that the Gray data changes, and the different illumination levels are resolved. The range of the photocurrents and, therefore, the range of illumination for which the ADC operates, can be adjusted by varying a primary clock frequency. The clock signal is modulated [Fig. 1(b)] in order to adapt the conversion range and to compensate for the inverse relationship between the photocurrent I_d and the pulse width T_d of the PWM sensor, shown in (1). In order to avoid large peak currents during the reset phase, each sensing voltage node (V_N) is asynchronously forced to V_c after the switching of the comparator. The charge-up current required to reset the sensing node is kept to a minimum as the proposed self-resetting operation prevents the total discharge of the sensing node using the SR latch. The charge–discharge swing is kept constant and equal to V_c–V_{ref} for all pixels within the array. A single Gray counter is used to generate the conversion data and feed them to the data bus of the on-pixel memories. The same bus is used in order to synchronously read out the pixel data during the scanning phase.

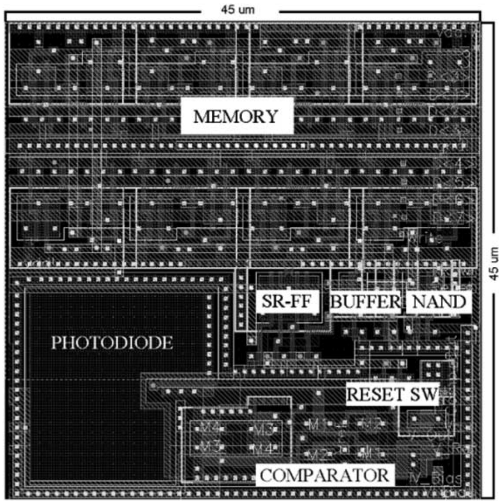

Fig. 2. Digital pixel layout occupying an area of 45 × 45 μm^2.

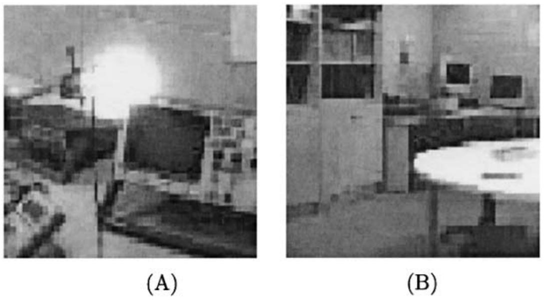

Fig. 3. Sample images acquired from the sensor.

III. EXPERIMENTAL RESULTS

To test and characterize its operation, the proposed digital pixel has been implemented in a prototype sensor array of size 64×64, which has been fabricated using a 0.35-μm CMOS process. Fig. 2 shows the layout of the pixel, which occupies an area of 45 × 45 μm^2. Fig. 3 shows two sample images acquired from the sensor. The array operates successfully with the ability to adapt the response of the pixel to different levels of illuminations. This adaptation principle is obtained by modulating up and down the clock frequency of the Gray counter, used to provide the data to the on-pixel memory, such that shorter and longer integration times are enabled, respectively. This adaptation process is illustrated in Fig. 4, which shows the experimentally measured integration times, detected by the DPS, as a function of the clock frequency of the Gray counter for five decades of illuminations. For a fixed frequency, the dynamic range is dictated by the 8-bit on-pixel memory (48 dB), however, by changing the clock frequency the inter-scene dynamic range is increased by over fiveorders of magnitude. The lower

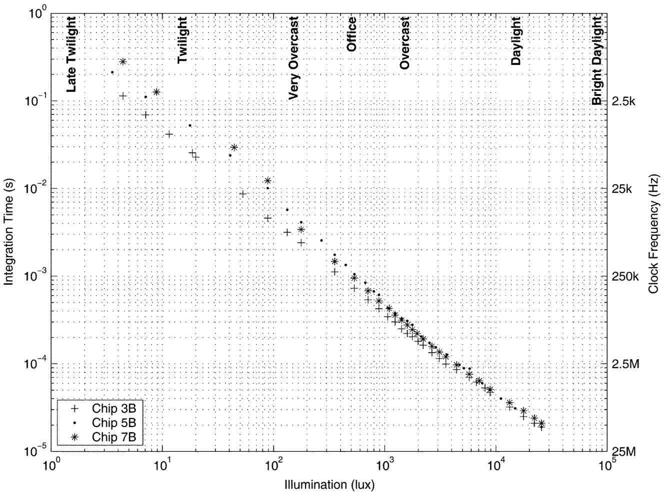

Fig. 4. Experimentally measured integration times as function of the clock frequency of the Gray counter and illumination.

TABLE I
MAIN FEATURES OF THE IMAGER

Features	Our PWM imager
Technology	CMOS $0.35\mu m$, 5M, 1P, 3.3V
Array size	64×64
Pixel size	$45 \times 45\mu m^2$
Fill-Factor	12%
Pixel's average current	$1.6\mu A$
Responsivity	$0.286 fA/\mu m^2/lux$
Dynamic range	85dB
Offset FPN	6.3 mV
Mean dark rate	9.8mV/s

limit is theoretically set by the dark current estimated at 1.68 pA. Even though the maximum available intensity level used in our experimental setup did not bring the sensor to saturation, an 85 dB operating range was still achievable with a clock frequency varying from 2 kHz to 25 MHz, as shown in Fig. 4.

The average current per DPS was measured at 1.6 μA. The resulting power consumption can be divided into three components: Power consumed by the digital circuit (memory and SR latch), power consumed by the chargeup of the sensing node, and finally power consumed by the analog comparator, representing 75%, 17%, and 8%, respectively. The charge-up power is kept quite low (17%) in our approach as the self-resetting operation, as proposed in this letter, prevents the total discharge of the sensing node using the SR latch. The charge–discharge swing is kept constant and equal to V_{c}–V_{ref} for all pixels within the array. Since an asynchronous reset approach is adopted, the power consumed is spread over time and large peak current typically experienced during the reset phase of conventional architecture is avoided. In addition, in contrast to the spiking pixel architecture [4], only a single pulse (PWM) is used in our approach in order to encode the photocurrent which results in further power saving. The average current of the spiking pixel was reported to be 132.8 μA per pixel with no on-pixel memory [4], compared to 1.6 μA of our sensor with on-pixel memory. Table I summarizes the performance of the manufactured chip.

IV. CONCLUSION

In this letter, we presented a digital vision sensor based on pulse width modulation scheme. An asynchronous self-resetting approach is implemented using a start integration signal instead of a global reset signal, avoiding large peak currents, encountered in a synchronous reset. In addition, the charge-up power is kept low (17%) as the proposed self-resetting operation prevents the total discharge of the sensing node using the SR latch. Each pixel within the array incorporates an analog processor as well as an on-pixel 8-bit memory and occupies an area of 45×45 μm^2. The array operates successfully with the possibility to adapt the response of the sensor to different levels of illumination: A programmable dynamic range is therefore achieved by simply modulating the clock signal of the timer.

REFERENCES

[1] S. Kleinfelder, S. H. Lim, X. Q. Liu, and El. Gamal, "A 10 000 frames/s 0.18 μm CMOS digital pixel sensor with pixel-level memory," in *Proc. ISSCC*, 2001, pp. 88–89.
[2] O. Yalid-Pecht and E. R. Fossum, "Wide intrascene dynamic range CMOS APS using dual sampling," *IEEE Trans. Electron Devices*, vol. 44, pp. 1721–1723, Oct. 1997.
[3] A. Bermak, A. Bouzerdoum, and K. Eshraghian, "A vision sensor with on-pixel ADC and in-built light adaptation mechanism," *Microelectron. J.*, vol. 33, no. 12, pp. 1091–1096, 2002.
[4] J. Doge, G. Schonfelder, G. T. Streil, and A. Konig, "An HDR CMOS image sensor with spiking pixels, pixel-level ADC, and linear characteristics," *IEEE Trans. Circuits Syst. II*, vol. 49, pp. 155–158, Feb. 2002.
[5] A. Uehara, K. Kagawa, J. Tokuda, T. Ohta, and M. Nunoshita, "Backilluminated pulse-frequency-modulated photosensor using silicon-onsapphire technology for use as epi-retinal prosthesis device," *Electron. Lett.*, vol. 39, no. 15, pp. 1102–1104, July 2003.
[6] E. Culurciello, R. Etienne-Cummings, and K. A. Boahen, "A biomorphic digital image sensor," *IEEE J. Solid-State Circuits*, vol. 38, pp. 281–294, Feb. 2003.