Silicon Photonics Scalable Design Framework: From Design Concept to Physical Verification

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The electronic IC market has benefitted greatly from the scalability attributed to Moore’s Law.

Meanwhile the photonic market remains limited to relatively small circuits.

Design differentiation still focused on device physics as opposed to novel device and sub-circuit re-use.

Objective: Scalable Photonics Design Infrastructure

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What is Required to Move Forward?

• Scalable Design Tools
  • Large scale optical simulation based on compact models
  • Automated/semi-automated layout
  • Physical verification and DFM

• Dedicated Process Development Kits (PDKs)
  • Pre-characterized compact models
  • Pre-characterized device pcells
  • Process specific PV and DFM decks
  • Validated tool settings

• Reference Flows
  • Validated design flows
  • Device characterization procedures
  • Test and measurement methodologies

• Validated Re-Usable IP?
Partnering to provide IoT Solutions

Photonic ICs
Physical Verification
Analog RF
Parasitic Extraction
3D/2.5D IC
Lithography Impacts
MEMS
Mask Data Preparation

Partners in Photonics

Partners in MEMS

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Mentor’s Custom IC Design Tools
Joint support for Pyxis and Tanner EDA Products

• Both utilize common PDK development utilities
  • Supports Python based PCells
  • Supports OA based PDK development

• Both support interface to Mentors “enterprise level” simulation and verification tools
  • Full support for Calibre® Physical Verification tools
  • Full support for Eldo Platform with Verilog-A support

• Tanner EDA will be fully OA native this year
  • L-Edit is Open Access native
  • S-Edit will be Open Access native in 17.2 release
Mentor’s Photonic IC Design Flow
Calibre’s Scalability with Tanner EDA platform

Native Open Access Design Environment

**Design Capture**
- **Tanner S-Edit**
  - Upcoming OA Native support in v17.2
  - Photonic SDL support
  - Supports Pre/Post-layout simulation

**Layout Implementation**
- **Tanner L-Edit**
  - Advanced Curves
  - X-Section
  - Photonic SDL Support
- **Luced IPKISS**
  - Photonic PCells
  - Waveguide generation
  - Layout direct simulation

**Comprehensive Open Access PDK Support**
- Luceda IPKISS PCells
- PyCell Studio PCells
- Future OA-API Plugins

**Photonic Simulation**
- **Luced CAPHE Simulator**
- **Future Photonic Simulation plugins**

**Electrical Simulation**
- Eldo Platform with Verilog-A support
- Tanner T-Spice with Verilog-A support

**Calibre RVE / Calibre Interactive**
- Lithography Simulation
  - Calibre LFD
- Design Verification
  - Calibre nmLVS
  - PERC, PERC LDL
- Photonic DRC and Chip Finishing
  - Calibre nmDRC, Calibre Yield

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Mentor’s Photonic IC Design Flow
Customer Driven

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Calibre RVE / Calibre Interactive
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Calibre Verification Platform
Physical Verification Challenges

• Rendered Curves Results in False DRC Errors

• Difficulty in LVS Device Recognition and Optical Property Comparison

• Need to Pass Waveguide Interconnect Extraction to Post-Layout Simulation

• Mask Generation and Silicon Manufacture Varies from Design Intent
DRC FOR NON-MANHATTAN PHOTONIC DESIGNS
DRC on Si-Photonics Components

Electronic IC (EIC) Layout (Manhattan Shapes)

Photonic IC (PIC) Layout (Non-Manhattan Shapes)

Design Shape
GDS

Curvilinear design:

Design shape
GDS

SEM images, Europractice

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Concentric arcs:

- Fabrication constraint:
  - Width > 1 µm, Space > 1 µm

\[
\begin{align*}
\text{Error}_{\text{width}} & := \text{width} < 1 \mu m \\
\text{Error}_{\text{space}} & := \text{space} < 1 \mu m
\end{align*}
\]

Traditional DRC Check

Number of Violations = 1500

Addressing DRC Photonics Challenges

I. False Error Induced by grid Snapping (2/2)

- Concentric arcs:
  - Fabrication constraint:
    - Width > 1 µm,
    - Space > 1 µm

```latex
\text{Error}_{\text{width}} := \text{width} < 1 \, \mu\text{m}
\text{Error}_{\text{space}} := \text{space} < 1 \, \mu\text{m}
```

Traditional DRC Check

New DRC Check using Calibre EqDRC

```
\text{All}_{\text{Thin}} := \text{Width} (\text{rod}) < 1 \, \mu\text{m}
W = \text{Width} (\text{Thin}_\text{rod}_{\text{width}})
\alpha = \text{Angle} (\text{Thin}_\text{rod}_{\text{width}})
L = \text{Length} (\text{thin}_\text{rod}_{\text{width}})
\text{If} (0 < \alpha < \text{max_angle}) \text{ OR } (L < \text{max_length}) \text{ Then:}
\text{Error}_{\text{rod}_{\text{width}}} := \text{Width}(\text{rod}) < (1 - \text{tol}) \, \mu\text{m}
\text{Else:}
\text{Error}_{\text{rod}_{\text{width}}} := \text{Width}(\text{rod}) < \text{max}_{\text{width}} \mu\text{m}
```

*.tol tolerance determined by applying tolerance factor according to fabrication grids and DRC rounding factors. (2sqrt(2). Grid)

Concentric Arcs with DRC violations


Number of Violations = 1500
Number of Violations = 145

DRC Post Processing using EqDRC capabilities
• **Taper test structure**
  • Taper is a trapezoidal shape.
  • End width (w) varies from .05 to 1 µm
  • Fabrication constraint :
    • Line width > 1 µm
    • For Robust strip design : relaxed width constraint with increased angle
Addressing DRC Photonics Challenges
II. Enable Multi-Dimensional Check (2/2)

Traditional DRC Rule (Complicated and non accurate)

Error_Width_1 := width < w1 when 0 < α < α₁
Error_Width_2 := width < w2 when α₁ < α < α₂
Error_Width_3 := width < w3 when α₂ < α < α₃

EqDRC Rule (Simple and Accurate)

α = Angle (rod)

α_critical = f(width(rod))

Thin_rod := αc/α > 1

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PHOTONIC LVS AND POST-LAYOUT SIMULATION
Photonic designers are used to a “Layout-centric” design flow. But as more complex and larger scale designs emerge, IC design flow-like methodology is required – “Schematic/Layout” design flow.

LVS to check if schematic and layout are equivalent

LVS equivalent:
- Circuit topology – Device type and count, Connectivity
- Device topology

Why Needed?

LVS check:
Are they equivalent?
LVS Overview

- Ensures the schematic of the design is equivalent with the layout
- Extraction Phase
  - Connectivity extraction
  - Device Extraction
  - Parameter Extraction
- Comparison Phase
  - Extracted design VS. Source design
  - Property Tracing
  - Discrepancy reporting
• Wild design shape
  • Non-Manhattan or curvilinear
• Extraction and careful validation required on non-traditional geometrical parameters:
  • Bend curvature
  • curvilinear path length
• Those properties can be context dependent
Litho Impacts on Silicon Photonics

• Optical Simulations Often do not Match Silicon Results
  • Litho simulation better captures ‘as manufactured’ structures

• Recommended Litho-Aware Device Characterization
  • Link to Lumerical Simulator improves device model parameters
  • Retargeting best practices to preserve intended topology
• Waveguide Bragg Grating Example
  • Ideal sharp edges of grating will smooth due to lithography resolution
  • This change in geometry will affect component attributes

• Modeled layout passed to simulation

• Litho Correction simulations match experimental Bragg bandwidth.

CONCLUSION
General Recommendations

- Need DRC decks dedicated for silicon photonics design
  - Cannot re-use decks targeted for IC design out of the box
  - Consider to add device shape-matching into DRC

- LVS checking for accuracy
  - Black-box devices for simple connectivity checking (shorts, opens)
  - Device shape matching (or push to DRC) for validation of pre-characterized device behavior

- Litho-simulation
  - Reduce mfg iterations through process modeling and simulation
  - Capture behavior impact through S-parameter update to optical simulation
  - Layout re-targeting or updated lithographic techniques to address outstanding issues
Growing Collaborations to provide “Full Scalable Si-Photonics Design Framework”

Mentor Graphics and Lumenerical Unify Optical Design and Simulation Flow

WILSONVILLE, Ore., September 19, 2014 – Mentor Graphics Corporation (Nasdaq: MENT), a leading supplier of electronic design automation, today announced a collaboration with Lumenerical to provide a unified framework that can be used to perform optical circuit simulations.

With this integration, users can take full advantage of the Mentor Graphics LRM™ and Lumenerical's Sipeed™ platforms, allowing for seamless data exchange and simulation capabilities. The collaboration will enable customers to leverage the latest technology for their optical design needs.

Lumenerical INTERCONNECT for Mentor Graphics

Optical circuit simulation within Mentor Graphics LRM™ can now be performed seamlessly alongside Lumenerical Sipeed™. This integration will enable design engineers to easily exchange data and results between the two platforms, streamlining the design process.

Full Scalable Si-Photonics Design Framework

The Full Scalable Si-Photonics Design Framework is a comprehensive solution for designing and simulating optical circuits on silicon photonics platforms. It includes a suite of tools that enable designers to accurately model and simulate optical components, ensuring optimal performance.

The framework includes:

1. Physical simulation and modeling tools for accurate prediction of device behavior.
2. Design flow that streamlines the entire design process, from concept to fabrication.
3. Integration with Mentor Graphics LRM™ for seamless data exchange.

Mentor Graphics and Luceda Photonics Deliver a PDK for imec's Integrated Silicon Photonics Platform

WILSONVILLE, Ore., March 20, 2017 — Mentor Graphics Corporation (Nasdaq: MENT) today announced, in collaboration with Luceda Photonics, the availability of a full flow process design kit (PDK) for imec’s Integrated Silicon Photonics Platform (ISIPP5G).

The PDK supports the Tanner IC design suite along with Tanner Calibre™ and Physical IC Design (Phys IC Design). Luceda’s IPKISS is integrated with Mentor’s L-Edit tool, providing a complete and integrated solution for optical design.

‘Ime’s ISIPP5G process technology is a key platform for silicon photonics companies,’ said Greg Lebsack, general manager of Tanner EDA at Mentor Graphics.

‘Delivering this PDK is significant for the market as it eliminates the manual, error-prone steps to establish a repeatable, efficient design flow. Now companies can get their innovative products to market more quickly and reliably using cost-effective tools and manufacturing.’

IPKISS is now integrated with L-Edit, giving photonic IC designers full control of their design framework to ensure they are up-to-date with the latest technology and trends in the industry.

‘Our customers ask for help automating the mechanics of design so they can use their skills and knowledge to deliver functionality, performance, and quality,’ said Pieter Dumon, CTO, Luceda. “The qualification of this PDK together with integration of IPKISS into the Mentor Tanner design flow delivers just that.’

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