Improve Chip Pin Performance Using Optical Interconnects

Zhehui Wang, Student Member, IEEE, Jiang Xu, Member, IEEE, Peng Yang, Student Member, IEEE, Xuan Wang, Student Member, IEEE, Zhe Wang, Student Member, IEEE, Luan Huu Kinh Duong, Student Member, IEEE, Zhifei Wang, Student Member, IEEE, Rafael Kioji Vivas Maeda, Student Member, IEEE, and Haoran Li, Student Member, IEEE

Abstract—With the fast development of processor chips, power-efficient, high-bandwidth, and low-latency interchip interconnects become more and more important. Studies show that the bandwidth of traditional parallel interconnects with low I/O clock frequencies will become bottlenecks in the near future. To solve this problem, two types of high-bandwidth interchip interconnects are developed. Low-swing differential electrical interconnects have widely been used in high-speed I/O designs. On the other hand, optical interconnects promise high bandwidth, low latency, and could improve the chip pin performance for manycore processors. They are becoming potential alternatives for electrical interconnects. This paper systematically models these two types of interconnects in terms of crosstalk noises, attenuation, and receiver sensitivities. Based on the proposed models, we developed optical and electrical interfaces and links (OEIL) and an analysis tool for OEIL. The OEIL can be used to analyze the energy consumption, bandwidth density, and latency of interconnects. Analytical models are verified by the results of published experiments. It shows that the optical interconnects have much higher bandwidth densities than the electrical interconnects. With this feature, the optical interconnects can significantly reduce I/O pin count compared with the electrical interconnects. For example, they can save at least 92% signal pins when connecting chips more than 25 cm (10 in) apart. The energy consumption of optical interconnects is comparable with that of electrical interconnects, and the latency of polymer waveguide-based optical interconnects is 18% less than that of electrical interconnect.

Index Terms—Interconnect, modeling, performance.

I. INTRODUCTION

In computing systems, the interconnect hierarchy can typically be divided into the following four categories: 1) cabinet level; 2) backplane level; 3) board level; and 4) chip level. Traditionally, interchip interconnects are installed on the printed circuit board (PCB) as parallel metal traces with low-frequency clocks. Since the number of I/O pins on chip package is limited by physical constraints, the total bandwidth of interchip interconnects is also limited. Because of the fast development of processor chips, such kind of interchip interconnect design could not meet the growing demand for communication bandwidth between chips, and will become a bottleneck in the near future. In high-performance computing systems, low power consumption, high bandwidth, and low latency interchip interconnects play increasingly important roles. Two types of interconnects are developed: 1) low-swing differential electrical transmission systems and 2) polymer waveguide- or fiber-based optical transmission systems.

Low-swing differential electrical transmission systems are widely used in computing systems. Peripheral component interconnect express (PCIe), serial advanced technology attachment, and universal serial bus are all high-speed serial interconnect interfaces in computers. For example, the PCIe v4.0 standard can support up to 16-Gbit/s data rate per lane [1]. In electrical interconnect, information is transmitted with two complementary signals on paired wires, and the receiver is able to obtain information from the voltage difference between these two wires. Since external interference affects both wires together, the crosstalk noises can effectively be reduced in the differential pair [2]. Optical transmission systems are promising candidates for high-speed interchip interconnects, and have been implemented in various labs. The transmission media can be fibers or polymer waveguides. For example, both the waveguide-based [3] and the fiber-based [4] interconnect can support over 10-Gbit/s data rate per waveguide or fiber. In optical interconnects, since signals at different wavelengths will not interfere with each other, the wavelength-division multiplexing (WDM) technology is developed, which multiplexes a number of signals with different wavelengths into a single waveguide or fiber.

To evaluate how optical interconnects could improve chip I/O pin performance for manycore processors, models are mathematically built for their crosstalk noises, attenuation, and receiver sensitivities, which are three important parameters for the analysis of interconnect performance. We develop optical and electrical interfaces and links (OEIL), an analysis tool for OEIL [5]. Assumptions of various parameters are made based on the state-of-the-art technologies, and the analytical results are already verified by published technical reports. Three parameters are used to compare the performance of...
interchip interconnects: 1) energy consumption; 2) bandwidth density; and 3) latency. Energy consumption is defined as the energy consumed by each interconnect when it transmits unit bits of information. Bandwidth density is defined as the total transmission bandwidth of a group of interconnects within unit geometry area. Latency is defined as the amount of time it takes for the head of signal to travel from the transmitter to the receiver. The differences between optical interconnects and electrical interconnects are studied in this paper.

The rest of this paper is organized as follows. Section II gives a survey of related work on the analysis and the comparison of electrical and optical interconnects. Section III introduces the basic structures and components of interchip electrical and optical interconnects. Section IV models them from the aspect of crosstalk noise, attenuation, and receiver sensitivity. Section V formulates their energy consumptions, bandwidth densities, and latencies. Section VI introduces OEIL (analysis tool), and quantitative analyzes and compares the performance of interchip electrical and optical interconnects. Finally, the conclusion is drawn in Section VII.

II. RELATED WORK

Comparisons have been done between optical interconnects and electrical interconnects. Cho et al. [6] compared interchip optical interconnects with electrical interconnects in terms of power and bandwidth. Chen et al. [7] compared on-chip waveguide-based optical interconnects with copper-based electrical interconnects in terms of latency, power, and bandwidth density. Feldman et al. [8] compared on-chip free space optical interconnects with electronic interconnects in terms of power and speed. Lee and Zhang [9] compared the on-chip free-space optical interconnect systems with fiber-based and Fresnel hologram optical interconnect systems in terms of power, latency and area. Berglind et al. [10] compared the power and signal-to-noise ratios (SNRs) of optical interconnects and electrical interconnects. In addition to them, some comparisons are done based on the simulations. Sellaye et al. [11] compared on-chip optical interconnects with electronic interconnects in terms of power and transmission throughput. Shin et al. [12] compared interchip optical interconnects with electronic interconnects in terms of data rate and power. Wang et al. [13] also discussed the related issues.

The power consumption, bandwidth, and latency of interconnects have been studied from different aspects. Bogatin [14] modeled the generic microstrip traces on the PCB board in terms of resistance, capacitance, inductance, and conductance. Ho et al. [15] studied the delay and bandwidth of on-chip electrical wires, which are fabricated under different technologies. Poon et al. [16] studied the power, bandwidth, and latency of optical switches based on cascaded microresonators (MRs). Miller [17] studied the density, energy, and timing issues of off-chip and on-chip optical interconnects. Different types of interchip optical interconnects were implemented. Ohashi et al. [18] introduced a cost-effective and low-power on-chip optical interconnect. A bonded structure of an Si-based optical layer is fabricated on a large-scale integration chip. Doany et al. [3] introduced terabit per second-class interchip optical interconnects based on a dense array of polymer waveguides.

This paper is compared with [6]–[9], which have worked on the performance analysis and modeling of optical interconnect. Models proposed in this paper are more holistic than the previous models. The differences are summarized in Table I, where the key parameters and configurations are listed. There are two marks in the table. If the parameter or configuration was modeled, it is marked by a check mark. If the parameter or configuration was discussed, but the exact models are not provided, it is marked by an asterisk mark. As shown in Table I, different from models in the previous work, the performance of optical interconnects is formulated in terms

<table>
<thead>
<tr>
<th>Parameter/Configuration</th>
<th>[5]</th>
<th>[6]</th>
<th>[7]</th>
<th>[8]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>1: Energy efficiency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1: Power consumption</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1: Transmitter power</td>
<td>✓</td>
<td>*</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.1: Crosstalk Noise</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.1.1: Number of Wavelength</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.1.2: Wavelength Spacing</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.1.3: MR Characteristics</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2: Optical Power Loss</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.1: Coupler Loss</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.2: Waveguide Attenuation</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.3: Interconnect Length</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.4: MR Characteristics</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.3: Receiver Sensitivity</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.3.1: PD Responsively</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.3.2: Signal to Noise Ratio</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.3.3: Modulation Frequency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.3.4: TIA Transimpedance</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.3.5: LA Sensitivity</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.4: Laser/Modulator Param.</td>
<td>✓</td>
<td>*</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.4.1: Threshold Current</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.4.2: Slope Efficiency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.4.3: Power Extinction Ratio</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.2: Receiver Power</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.1: TIA Power</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.1.1: PD Input Capacitance</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.1.2: Signal Frequency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.1.3: TIA Supply Voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.2: LA Power</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.2.1: LA Supply Current</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.1.1.2.2.2: LA Supply Voltage</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>1.2: Data Rate</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2: Bandwidth Density</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2.1: Data Rate per Wavelength</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2.2: Number of Wavelengths</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2.2.1: MR Characteristics</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2.2.2: Wavelength Spacing</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2.3: Optical Pin Pitch</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>2.4: Waveguide Pitch</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>3: Latency</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>3.1: RC Delay</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>3.2: Propagation Delay</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>3.2.1: Interconnect Length</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>3.2.2: Signal Propagation Speed</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

* Parameters are discussed but not modeled

MR = Microresonator  TIA = Transimpedance Amplifier
PD = Photodetector  LA = Limiting Amplifier
of the basic parameters and configurations in this paper. This model covers the key factors of interconnect performances, especially on crosstalk noises, optical power losses, as well as receiver sensitivities. A clear insight of optical and electrical interchip interconnects is given in this paper.

III. BACKGROUND

In this section, the background of electrical interchip interconnects and optical interchip interconnects is introduced. Their structures include transceivers, package pins, and transmission medium. These components are compared from different aspects. These two types of interchip interconnects will be modeled in Section IV.

A. Overview

The basic structure of electrical interconnects is shown in Fig. 1(a). On the transmitter side, input signals are amplified by a multistage preamplifier. They are processed by the driver, which outputs current to drive the interconnect. The driver is connected to the electrical pin. On the receiver side, signals are transmitted from the electrical pin. They are processed by the equalizer, which can reverse the distortion phenomenon that one bit signal interferes with subsequent bits. Signals are detected and amplified by the limiting amplifier. The basic structure of optical interconnects is shown in Fig. 1(b). On the transmitter side, the electrical signals are processed by the preamplifier and the driver, which outputs current to drive the laser. Electrical signals are converted into optical signals and coupled into the optical pin. On the receiver side, optical signals are transmitted through the optical pin. The photodetector receives optical signals, and generates currents based on power intensities. The transimpedance amplifier converts current signals into voltage signals, which are detected and amplified by the limiting amplifier.

B. Transceiver

The schematic of electrical transceiver is shown in Fig. 2, which includes the driver, the two differential traces, and the limiting amplifier [19]. The driver consists of two nMOS transistors, two pull-up resistors, and a current source.

The differential input pair $V_{in}$ is connected to the gates of two transistors. At any time, only one transistor is in ON-state, and current $2I_0$ flows through that transistor. The current $2I_0$ comes from two directions. A portion of the current comes from the power supply and the rest of current comes from the traces. The current directions are shown by arrows in the schematic. On the receiver side, there are two pull-up resistors connected to the limiting amplifier. At any time, the current flows through only one pull-up resistor. Therefore, the two input ports of the limiting amplifier have different voltage levels. This voltage difference can be detected and amplified to output pair $V_{out}$. The input voltage $V_{in}$ is either positive or negative to represent signal logic level 0 or 1. As a result, the output voltage $V_{out}$ is either positive or negative.

The schematic of optical transceiver is shown in Fig. 3. The transmitter, also called electrical-to-optical interface, includes a laser driver and a laser diode. The laser driver is similar to the driver in electrical interconnects. If the left transistor is in ON-state, current $I_{mod}$ flows through the pull-up resistor and current $I_{bias}$ flows through the laser diode. If the right transistor is in ON-state, both currents $I_{mod}$ and $I_{bias}$ flow through the laser diode. Therefore, the laser diode has two output power levels, which represent signal logic level 0 and 1, respectively. The receiver, also called optical-to-electrical interface, includes a photodetector, a transimpedance amplifier, and a limiting amplifier. When the photodetector receives light, its output current is proportional to the light intensity. This current is converted into voltage by the transimpedance amplifier. The limiting amplifier compares this voltage with a constant voltage. Because the output power of laser diode has two levels, the photodetector will receive optical signals in two different intensities.
Loss is related to loss tangents $\tan\sigma$ can be used in the PCB, such as FR-4, RO4003. The signal planes. Compared with microstrips, striplines can eliminate the dispersion is low in short-range signal and increase its important parameter of electrical pins, which attenuates the signal and increase its $RC$ delay. Normally, the resistance of pin is matched with the characteristic impedance of metal trace, so that the power transfer efficiency is maximized, and the reflection from the interconnect is minimized.

Optical pins are used as data interfaces among packages. For power supply and ground pins, the electrical interfaces are used. Optical pins connect polymer waveguides or fibers with the transmitter or the receiver. It could be lenses [3] or grating couplers [21]. They are arranged in a grid on the top or at the bottom of the package. Similar to electrical pins, the bandwidth density of the package is related to the pitch of optical pins. The coupling loss is defined as the power loss that occurs when optical signal is transmitted through optical pins. Optical signals do not have $RC$ delays, but will be degraded by refractive losses. The dispersion is low in short-range single-mode waveguide or fiber [22].

D. Transmission Media

In electrical interconnects, striplines are implemented as transmission media. The cross section of striplines is shown in Fig. 4. The traces are fabricated between two ground planes. Compared with microstrips, striplines can eliminate the forward crosstalk noises [23]. Different types of materials can be used in the PCB, such as FR-4, RO4003. The signal loss is related to loss tangents $\tan\sigma_D$, whose value is different in different materials. The distance between two ground planes is $H$, and the height of each trace is $h$. The trace width and the spacing between two traces of one differential pair are assumed to be $w$. Pitch $p_e$ is defined as the spacing between two nearby differential pairs. An industry toolkit called Saturn PCB Design [24] following standard IPC-2152 [25] is used to calculate the direct current resistance $R_{DC}$, the characteristic impedance $Z_0$, and the capacitance per-unit length $C_0$.

In optical interconnects, polymer waveguides or fibers are implemented as transmission media. It is assumed that the WDM technology is used. Signals at different wavelengths could be transmitted in one single waveguide or fiber. The number of wavelengths in one interconnect is $m_o$, and the attenuation coefficient of interconnect is $\alpha_o$, which describes the energy loss rate of optical signals transmitted in interconnect with the unit length. Polymer waveguides could be fabricated into multiple layers. In a single layer, parallel waveguides are fabricated. Pitch $p_o$ is defined as the spacing between two neighboring polymer waveguides. MRs are used to couple optical signals into waveguide, and they can also filter signals with specific wavelengths out of waveguide [26]. The transmission media of optical interconnect could also be fibers.

IV. INTERCHIP INTERCONNECT MODELING

In this section, models for low-swing current-mode differential electrical interconnects, and WDM optical interconnects are built. The crosstalk noise, the attenuation, and the receiver sensitivity of these two transmission systems are analyzed and compared. The performance of interconnects will be analyzed in Section V.

A. Crosstalk Noise

In electrical interconnects, the crosstalk coefficient is defined as the ratio of noise amplitude to signal amplitude. Compared with single-ended traces, the crosstalk noise in differential traces is relatively small [2]. The near-end crosstalk noise (NEXT) among parallel traces on board is the main source of crosstalk noise. This is because for properly terminated low-loss striplines, the far-end crosstalk noise (FEXT) is relatively very low [23]. We define $c(d)$ to be the crosstalk coefficient between two parallel traces with distance $d$, and it is expressed in

$$c(d) = H^2/(4d^2 + H^2).$$  \hspace{1cm} (1)

In (1), $H$ is the distance between two metal layers, as shown in Fig. 4. Parallel differential traces on the PCB board are analyzed, and the cross-sectional view is shown in Fig. 5. The crosstalk coefficient between the differential pair $n$ and $n + i$ is expressed in

$$N_d(i) = c(|i|p_e - 2w) - 2c(|i|p_e) + c(|i|p_e + 2w).$$  \hspace{1cm} (2)

The victim trace pair $n$ has two traces in opposite directions, and the aggressor trace pair $n - 1$ also has two traces in opposite directions. Therefore, the crosstalk coefficient between two trace pairs is the summation of four terms. Apart from trace pair $n - 1$, there are other aggressor trace pairs, such as $n + 1$ and $n + 2$. The total coefficient $\varepsilon_e$ is expressed in

$$\varepsilon_e = \cdots + N_d(-1) + N_d(1) + N_d(2) + \cdots$$  \hspace{1cm} (3)

It is assumed that there are $m_e$ parallel trace pairs on the PCB board. The trace pair located in the middle of those
It is assumed that there are \( m_o \) different wavelengths in WDM optical systems. The spacing between two neighboring wavelengths is \( \Delta \lambda \), and it is assumed to be 1.8 nm. The crosstalk noise coefficient of optical interconnects is maximized when \( n \) equals to \( \lfloor m_o/2 \rfloor \), and it is expressed in

\[
\varepsilon_o = 2 \sum_{i=1}^{\lfloor m_o/2 \rfloor} T_d(\lambda_n + i \Delta \lambda). \tag{8}
\]

### B. Attenuation

In electrical interconnects, trace attenuation \( A_e \) is the ratio of output signal amplitude to input signal amplitude, and is expressed in (9). \( \alpha_e \) is the attenuation coefficient of trace and \( L \) is the interconnect length. In addition, \( \eta_e \) is the attenuation of each electrical pin, and there are two pins in a single electrical interconnect

\[
A_e = \eta_e^2 e^{-\alpha_e L}. \tag{9}
\]

The attenuation coefficient \( \alpha_e \) is expressed in (10), where the first and the second terms are called skin-effect loss and dielectric loss [26], respectively. In striplines, \( w \) and \( h \) are the width and the height of trace, as shown in Fig. 4. \( R_{dc} \) is the direct current resistance, \( Z_0 \) is the characteristic impedance, and \( C_0 \) is the capacitance per-unit length. \( \tan \delta \) is the loss tangent in dielectric material. Their values will be discussed in Section VI. In addition, \( f_s \) is the frequency when skin depth equals half of trace height \( h \), which is 13.8 MHz. \( f \) is the working frequency of the signal. The attenuation coefficient is increased, if \( f \) is increased

\[
\alpha_e = R_{dc}(w + h) \left( \frac{f}{f_s} \right)^{0.5} + \pi f C_0 \tan \delta Z_0. \tag{10}
\]

The current in electrical interconnects will drive the electrical pins on both sides of the trace, as shown in Fig. 2. After infinite time, the voltage on the pin will be driven to the full swing voltage. However, for each bit signal, the time to drive the pin is half of the period \( 1/f \). The ratio of the voltage after that given time to the full swing voltage is defined as the attenuation of each pin \( \eta_e \), and it is expressed in (11). To drive the pin, current will be attenuated by resistance \( Z_0 \) and capacitance \( C_p \) of electrical pin. In this model, the capacitance of pin \( C_p \) is assumed to be 0.5 pF [29]

\[
\eta_e = 1 - e^{-\frac{1}{2Z_0C_p}}. \tag{11}
\]

In optical interconnects, attenuation \( A_o \) is defined as the ratio of received optical power to transmitting power. It includes the coupling loss of optical pins, the passing by and insertion loss of MRs, and the attenuation of waveguides or fibers. It is expressed in

\[
A_o = \eta_o^2 e^{-\alpha_o L_p (m_o - 1) T^2_d(\lambda_n)}. \tag{12}
\]

In (12), \( \eta_o \) is the coupling efficiency of each optical pin, which works as the interface between the transceiver and the waveguide. \( \alpha_o \) is the attenuation coefficient of waveguide. In this model, \( \eta_o \) and \( \alpha_o \) are assumed to be 0.69 and \(-0.0276/\text{cm}\), respectively [3]. In addition, \( L_p(n) \) is the passing
by loss, and $T_d(\lambda)$ is the insertion loss of each MR. There is one MR after the laser and another one MR before the photodetector.

Optical signals will be attenuated if they pass by MRs. For example, in Fig. 8, signal $\lambda_n$ will be attenuated by a sequence of MRs, whose resonance wavelengths range from $\lambda_0$ to $\lambda_{n-1}$. The ratio of the pass port power to the input port power is a function of light wavelength. The pass port transmission spectrum is expressed in (13). Parameters, such as $a$, $r$, and phase shift $\theta(\lambda)$, have been discussed in Section IV-A

$$T_p(\lambda) = \frac{r^2a^2 - 2r^2a \cos \theta + r^2}{1 - 2r^2a \cos \theta(\lambda) + r^4a^2}. \quad (13)$$

The pass port spectrums of two of the MRs are shown in Fig. 9. At their resonance wavelengths $\lambda_{n-2}$ and $\lambda_{n-1}$, the value of $T_p$ is minimized. At other wavelength, the attenuation factor is close to one. The total passing by loss is expressed in (14), where $T_p(\lambda)$ is the frequency spectrum of MR with resonance wavelength $\lambda_n$, and $\Delta \lambda$ is the spacing between two neighboring wavelengths. In the worst case scenario, the passing by loss reaches its maximum point when $n$ equals to $m_o - 1$, where parameter $m_o$ is the total number of optical wavelengths in one waveguide. In this model, it is assumed that $a = 0.9993$, $k = 0.3$, $n_e = 2.65$, and the radius $R$ is $\sim 10 \mu m$ [16]

$$L_p(n) = \prod_{i=1}^{n} T_p(\lambda_n + i \Delta \lambda). \quad (14)$$

C. Receiver Sensitivity

Sensitivity is defined differently in electrical and optical receivers. In electrical interconnects, shown in Fig. 2, the driver injects currents through the pair of differential traces, and induces a voltage difference between the two ports of limiting amplifier [30]. Only when this voltage difference is less than $-V_{th}$ or greater than $+V_{th}$, it could be detected. (b) When the BER equals to $10^{-12}$, logic 1 and logic 0 voltage levels are $\pm 7\sigma$ away from the theoretical decision point in the middle. (c) Theoretical decision point needs to be opened by at least double the threshold voltage $2V_{th}$ of the limiting amplifier.

In optical interconnects, shown in Fig. 3, the sensitivity of optical receiver is the minimum optical modulation amplitude (OMA) required in the receiver end, which is defined as the difference between two optical logic power levels from the optical source [31]. In this paper, the minimum voltages difference required on the two input ports of limiting amplifier is first analyzed. One port of the limiting amplifier is connected to the output of transimpedance amplifier, and its probability distribution of voltages is shown in Fig. 10.

It is assumed that the noise is Gaussian distributed with standard deviations $\sigma$. Fig. 10(b) shows the region overlapping where the bit error rate (BER) equals to $10^{-12}$, the SNR equals to 14.1, and logic 1 and logic 0 voltage levels are $\pm 7\sigma$ away from the theoretical decision point in the middle. The limiting amplifier itself has a threshold voltage. If the voltage difference of the two ports is less than the threshold voltage, the electrical signal cannot be detected by the amplifier. The theoretical decision point is opened by at least double the threshold voltage $2V_{th}$ of the limiting amplifier, as shown in Fig. 10(c)

$$OMA = \frac{i_n 0.5 \cdot SNR + 2V_{th}Z_{th}^{-1}}{\rho}. \quad (15)$$
The OMA is expressed in (15). \( i_n \) is the input referred rms noise density of the transimpedance amplifier, which is assumed to be 10 pA/\( \sqrt{\text{Hz}} \). In addition, \( Z_{\text{th}} \) is the transimpedance, and \( \rho \) is the responsivity of photodetector. In this model, their values are assumed to be 1 k\( \Omega \) and 1 A/W, respectively.

V. Performance of Interchip Interconnect

In this section, the performance of electrical and optical interconnects is analyzed in terms of energy consumption, bandwidth density, and latency based on Section IV. The model in this paper is applicable to various electrical and optical interchip interconnects with different devices, and the formulations are general to different technologies.

A. Energy Consumption

The overview structure of electrical interconnects is shown in Fig. 1(a). The energy consumed by preamplifier and equalizer is ignored. The total power consumption is expressed in (16). Current \( I_0 \) is the supply current of the driver, \( I_{\text{th}} \) is the supply current of the limiting amplifier, and \( V_c \) is the supply voltage of these two components. The supply voltage \( V_c \) is assumed to be 1.5 V. The value of \( I_{\text{th}} \) is approximately proportional to the working frequency of limiting amplifier, and is assumed to be 0.3 mA for 1-GHz frequency. For example, at 10-GHz working frequency, the supply current of limiting amplifier is 3 mA

\[
P_c = (2I_0 + I_{\text{th}})V_c. \tag{16}
\]

The noise margins on input ports of limiting amplifier are shown in Fig. 11(a). The received electrical signal has two voltage levels named \( V_l \) and \( V_0 \), which represent logic levels of 1 and 0. In Fig. 11(a), \( A_e \) and \( \epsilon_e \) are the attenuation and the crosstalk noise coefficient of electrical interconnect, respectively. Their values have been discussed in Section IV. \( \epsilon_e \) is called the transmitter offset coefficient, which is defined as the ratio of offset amplitude to signal amplitude, and it is assumed to be 0.05 in this model. The minimum required eye amplitude in electrical interconnects is \( A_e - \epsilon_e - \epsilon_c \), which corresponds to \( V_{\text{th}} \) and the sensitivity of electrical receivers. The minimum supply current required from the driver is double the current \( I_0 \), which is expressed in (17). \( Z_d \) is the differential impedance between two inputs of the differential pair, and the value is 104 \( \Omega \) based on the tool

\[
I_0 = \frac{2V_{\text{th}}}{(A_e - \epsilon_e - \epsilon_c)Z_d}. \tag{17}
\]

The overview structure of optical interconnects is shown in Fig. 1(b). The energy consumed by preamplifier and equalizer is ignored. The total power consumption is expressed in (18). Current \( I_{\text{mod}} \) and \( I_{\text{bias}} \) are the supply current and bias current of laser driver, and \( I_{\text{th}} \) is the supply current of transimpedance amplifier. The supply voltage required by the laser is greater than the voltage required by electrical components. \( V_l \) is the supply voltage of laser. In this model, its value is assumed to be 3 V

\[
P_o = (I_{\text{mod}} + I_{\text{bias}})V_l + (I_{\text{th}} + I_{\text{th}})V_c. \tag{18}
\]

The noise margins on the input port of photodetector are shown in Fig. 11(b). The received optical signal has two power levels named \( P_l \) and \( P_0 \), which represent logic levels of 1 and 0. \( \epsilon_o \) is the crosstalk noise coefficient in optical interconnects. Extinction ratio \( r_e \) is defined as the power ratio between logic level 0 and logic level 1, and it is assumed to be 0.1 in this model. The minimum required eye amplitude in optical interconnect is \( 1 - \epsilon_o - r_e \), which corresponds to the OMA, the sensitivity of optical receiver. The minimum driving current required from the laser is the summation of supply current and bias current, and it is expressed in (19). \( A_o \) is the total attenuation of entire optical interconnect. On the receiver end, different from electrical ones, noises in optical interconnects have also been attenuated. In addition, \( \eta_l \) and \( I_{\text{th}} \) are the slope efficiency and the threshold current of laser diode, respectively. In this model, they are assumed to be 0.2 W/A and 1 mA, respectively [32]

\[
I_{\text{mod}} + I_{\text{bias}} = \frac{\text{OMA}}{A_o(1 - \epsilon_o - r_e)\eta_l} + I_{\text{th}}. \tag{19}
\]

The supply current of transimpedance amplifier is proportional to the input pole of transimpedance amplifier, and it is expressed in (20). \( C_{\text{pd}} \) is the input capacitance of photodetector, which typically equals to 60 fF [33], and \( \Delta V \) is the saturation voltage of the transistor in transimpedance amplifier, which is assumed to be 0.1 V

\[
I_{\text{th}} \approx \pi f C_{\text{pd}} \Delta V. \tag{20}
\]

The power consumption of either electrical signals or optical signals is the function of its transmitting bandwidth. Since electrical interconnects and optical interconnects work on different frequencies, it is not proper to compare them directly. Alternatively, their energy consumptions are evaluated and compared. The energy consumption is defined as the energy consumed by interconnects when they transmit one bit of information. Based on the definition, if both signals transmit the same amount of bits, the interconnect which consumes less energy has a smaller value of energy consumption. The energy consumption is expressed in

\[
\text{Energy Consumption} = \frac{\text{Power} P}{2 \cdot \text{Frequency} f}. \tag{21}
\]
In (21), \( P \) is power consumption of either electrical signals or optical signals. The working frequency of signal is \( f \), so that the signal bandwidth is \( 2f \) if nonreturn to zero code is applied. In electrical interconnects, each signal is transmitted by an independent differential trace pair. In optical interconnects, each signal has its unique wavelength, and does not interfere with other signals in the same waveguide. Hence, the energy consumption of each signal equals to the energy consumption of the entire interconnect.

B. Bandwidth Density

In electrical interconnects, there is only one signal in each differential pair. Therefore, the bandwidth of each electrical interconnect equals double the frequency, \( 2f \). If the signal frequency is increased, the trace attenuation is increased. The value of coefficient margin \( \Delta c \), expressed in (22), will be decreased. It is possible that these signals will not be detected by the receiver because of noises. Every receiver has a minimum required coefficient margin, and the signal frequency of electrical interconnects is limited. Parameters \( \varepsilon_e \) and \( \varepsilon_c \) have been discussed in Section V-A

\[
A - \varepsilon_e - \varepsilon_c = \Delta c. \tag{22}
\]

In (22), \( \Delta c \) is the coefficient margin, which is assumed to be 0.01 in this model. As mentioned in Section IV, the attenuation coefficient \( \alpha_e \) is the function of working frequency \( f \), and this relationship could be expressed as \( \alpha_e = A(f) \). Function \( A \) is a monotonically increasing function, and its inverse function is \( A^{-1} \). The maximum bandwidth of a single electrical interconnect is the function of trace length, which is expressed in (23). It can be seen that if the interconnect length is increased, the bandwidth of electrical interconnects will be decreased

\[
B_e = 2A^{-1}\left(-\frac{\ln(\varepsilon_e + \varepsilon_c + \Delta c)}{L}\right). \tag{23}
\]

In optical interconnects, there could be multiple signals in one interconnect. The number of signals in one interconnect equals the free-spectral range (FSR) divided by the spacing between two neighboring wavelengths. As shown in Fig. 7, FSR is defined as the spacing between two successive resonance peaks in drop port or pass port spectrum, and its value is expressed in (24). Parameters \( \lambda \), \( R \), and \( n_e \) have been discussed in Section IV

\[
\text{FSR} = \frac{\lambda^2}{2\pi n_e R}. \tag{24}
\]

The bandwidth of each optical interconnect equals to the transmission bandwidth of one optical signal multiplied by the number of signals in one interconnect, and it is expressed in (25). \( \Delta \lambda \) is the wavelength spacing between two neighboring signals, which is assumed to be 1.8 nm in this model. The transmission bandwidth of each signal is also double the working frequency, \( 2f \). Different from electrical interconnects, the bandwidth of optical interconnects is not limited by the transmission distance, but is related to the speed of EO/OE interfaces. The maximum bandwidth of optical interconnects depends on the performance of electrical components. A constant value of bandwidth is assumed in optical interconnects, which is close to the maximum transmission bandwidth of electrical interconnects

\[
B_o = 2 \left\lfloor \frac{\text{FSR}}{\Delta \lambda} \right\rfloor f. \tag{25}
\]

Both electrical and optical pins are located on the chip package. At the bottom of package, there are a grid of pins, as shown in Fig. 12(a). It is assumed that each single interconnect has the same transmission bandwidth, and the total transmission bandwidth is proportional to the package area. The area bandwidth density is defined as the maximum bandwidth in unit area, and is expressed in (26). It is a parameter to evaluate the data throughput through the chip package

\[
\text{Area Density} = \frac{\text{Bandwidth } B}{\text{Area } S}. \tag{26}
\]

In (26), \( B \) is the bandwidth of each single interconnect, and \( S \) is the pin area. In electrical interconnects with the Fineline BGA package [34], the distance between two neighboring pins is \( \sim 1 \) mm, and the area \( S_e \) equals to 1 mm\(^2\). The area of each pin in the Micro Fineline BGA package is \( \sim 0.25 \) mm\(^2\). In optical interconnects, it is assumed that the size of each pin is \( 250 \) \( \mu \)m \( \times \) 250 \( \mu \)m [4], and the area \( S_o \) equals to 0.063 mm\(^2\).

Both electrical and optical interconnects are fabricated in multiple layers. In each layer, there are parallel interconnects, as shown in Fig. 12(b). It is assumed that each single interconnect has the same bandwidth, and the total transmission bandwidth is proportional to the layer width. The linear bandwidth density is defined as the maximum bandwidth in unit width, and is expressed in (27). It is a parameter to evaluate the data throughput through interconnects

\[
\text{Linear Density} = \frac{\text{Bandwidth } B}{\text{Pitch } p}. \tag{27}
\]

In (27), \( p \) is the interconnect pitch. In electrical interconnects, pitch \( p_e \) equals to the distance between two neighboring differential trace pair plus the pair width. In optical interconnects, pitch \( p_o \) equals to the distance between two neighboring waveguide plus the waveguide width. The multilayer linear bandwidth density equals to the single-layer linear bandwidth density multiplied by the number of layers in the PCB board.
C. Latency

The latency of interchip interconnects is the amount of time it takes for the head of signals to travel from the transmitter to the receiver. In either electrical interconnects or optical interconnects, the input and output signals are electrical signals. Their waveforms are described in Fig. 13. Interconnect latency is defined as the time required for the output signal to reach half of its final output level after the moment that the input signal changes to half of the input level. It includes two parts, propagation delay and \( RC \) delay. The propagation delay is proportional to the interconnect length, and is inversely proportional to the signal speed.

In stripline design, copper traces on the PCB board are surrounded by the dielectric material. When an electrical signal propagates along the trace, its speed is determined by the speed of a changing electric and magnetic field, which is in fact the speed of light in the material [23]. The propagation speed of electrical signals is related to the relative dielectric constant of that material, and is expressed in

\[

v_e = \frac{c}{\sqrt{\epsilon_r}}.

\]  

In (28), \( c \) is the light speed in vacuum, which is \( \sim 12 \) in/ns. \( \epsilon_r \) is the relative dielectric constant of the material in the PCB board, and the values of \( \epsilon_r \) are different in different PCB boards. For example, \( \epsilon_r \) equals to 3.6 in RO4003 board [35] and equals to 4 in FR4 board [36]. The signal speed is inversely proportional to the square root of the relative dielectric constant.

In optical waveguides or fibers, it is assumed that signals have a long pulse with narrow bandwidth, and their nonlinear effects are ignored. The speed of optical signals is determined by their group velocities, with which the envelope of a pulse propagates in the optical medium [37]. The propagation speed of optical signals is related to the group refractive index of that medium, and is expressed in

\[

v_o = \frac{c}{n_g}.

\]  

In (29), \( n_g \) is the group reflection index of optical interconnect, and the values of \( n_g \) are different in different optical transmission media. For example, \( n_g \) equals to 1.55 in polymer waveguide [38], and equals to 1.47 in a single-mode optical fiber [22]. The signal speed is inversely proportional to the refractive index.

When electrical or optical signals are transmitted from the transmitter to the receiver, they will pass several electrical modules, as shown in Fig. 1. In addition to propagation delay, the parasitic capacitances of these electrical modules will also generate delays, and such kind of delays is called \( RC \) delays. If the \( RC \) delay is too large, signals will be distorted, in which one bit interferes with subsequent bits. This phenomenon is called intersymbol interference, and could be reduced by equalizers [30]. Therefore, the value of \( RC \) delay cannot exceed one bit period \( 1/2f \). Finally, the interconnect latency is expressed in (30). \( v \) is the signal propagation speed, and \( \tau_{RC} \) is the \( RC \) delay of electrical modules

\[

\text{Latency} = \frac{\text{Length} L}{\text{Speed} v} + \text{Delay} \tau_{RC}.

\]  

VI. QUANTITATIVE ANALYSIS AND COMPARISON

In this section, the analytical models are verified. The performance of electrical and optical interconnect is calculated and compared by an analysis tool OEIL. It is possible that the values of parameters will vary due to the differences of technologies. This analytical model will still be effective in these situations.

A. Analysis Tool OEIL

We develop OEIL, an analysis tool for optical and electrical interfaces and links. Fig. 14 shows the internal structure of OEIL. The publicly released OEIL is implemented in C code, and it is available online with documentation at [5]. OEIL has a complete library of devices for interchip
The article analyzes power consumptions, energy efficiencies, bandwidths, bandwidth densities, and latencies of optical and electrical interchip interconnects. As shown in the figure, the main body of OEIL includes models for crosstalk noises, attenuations, receiver sensitivities, power consumptions, bandwidths, and latencies. This tool is designed based on the proposed analytical models in Section V. The input files of tool OEIL include interconnect configurations and device parameters, and the output results are written in output. The configurations of interconnects, such as data rate, interconnect length, and number of parallel interconnects, are described in file interconnect configurations. The parameters of board, MR, trace, waveguide, transmitter, and receiver can be found in file device parameters. Those files have two versions, which are differenced by key words electrical and optical. In addition to the above results, OEIL also generates the intermediate results of analytical models, such as crosstalk talk coefficients, attenuations, and receiver sensitivities.

OEIL evaluates the performance of interchip interconnects from end to end, which consists of on-chip interconnect, off-chip interconnect, and interfaces between them. For electrical interconnects, the device library includes the parameters of wires on chip, traces on board as well as electrical copper pins. For optical interconnects, the device library includes the parameters of silicon waveguides on chip, polymer waveguides on board, and optical lens or couplers. In addition, OEIL is also able to evaluate the performance of interchip interconnects, which connect 2.5-D or 3-D chips. The device library includes the parameters of through-silicon vias and bumps among stacked dies. Configurations of the 2.5-D or 3-D chip can be defined on the configuration file. This tool OEIL is able to not only analyze the performance of interchip interconnects but also provide necessary parameters for system simulators. The configuration file is able to describe all kinds of interconnects in a network. OEIL is verified by the data from the previous published technical reports. It shows good fitting between the OEIL and the collected data. The verification will be discussed with more details in Section VI-B. By updating the device library, OEIL is able to follow the development of technologies.

Fig. 15. Maximum bandwidth of electrical interconnect is plotted. It shows that this analytical model could match the experiment results well.

Fig. 16. When the frequency or the interconnect length is increased, the energy consumption of electrical interconnect is rapidly increased.

Fig. 17. When the frequency or interconnect length is increased, the energy consumption of optical interconnect is gradually increased.

B. Verification

Assumptions of various parameters are made based on the state-of-the-art technologies. For electrical interconnects, the geometry of traces is assumed according to the typical design of multilayer board [39]. In this model, \( H \) is assumed to be 17.4 mil (0.44 mm), \( h \) is assumed to be 1.4 mil (0.04 mm), and \( w \) is assumed to be 4 mil (0.10 mm). \( p_e \) is assumed to be 24 mil (0.61 mm), and \( m_e \) is assumed to be 8. On the other hand, for optical interconnects, the geometry of waveguides is assumed based on an IBM prototype [4]. In this model, \( p_o \) is assumed to be 62.5 \( \mu \)m [3], and \( m_o \) is assumed to be 8. Other parameters have been discussed in Section IV and Section V. It is possible that some of the parameters change because of the advancement of technologies, and the comparison results between them are different. This model has wide effective ranges, and the calculation results can be updated with new parameters. In this section, the model of electrical interconnects will be verified by the previous experiments.

The model is verified by showing the maximum bandwidths of electrical interconnects in Fig. 15. In this chart, the curve is plotted based on this model, and the stars are plotted based on the experiment results. In the analytical model, the relationship between the maximum bandwidth of interconnects and the interconnect length is obtained from (23). In the experiment, traces with specific length are fabricated on the board first. The bandwidth of each trace pair is then increased until
transmitted data cannot be read correctly by the receiver. The final bandwidth is recorded as the maximum bandwidth of interconnects with that given length. We collect the experiment results from published technical reports [40]–[43]. The plots show that this analytical model could match experiment results well. In electrical interconnects, the maximum bandwidth and the maximum interconnect length are limited. If the interconnect length is increased, the bandwidth has to be decreased. Similarly, if the data bandwidth is increased, the interconnect length has to be decreased.

C. Energy Consumption

The energy consumptions of electrical and optical interconnects are plotted in Figs. 16 and 17. The length of interchip interconnects is typically less than 100 cm (40 in) [6], and the bandwidth is typically greater than 10-Gbit/s data rate. In these calculations, it is assumed that the frequency of signals ranges from 5 to 60 GHz, and the total energy consumption includes the power consumption of the transmitter, the interconnect itself, and the receiver. In real high-speed interchip interconnects, in order to cope with the slow speed of data sources, there is a serializer implemented before the transmitter and a deserializer implemented after the receiver. Since serializer and deserializer are both implemented in electrical interchip interconnects as well as optical interchip interconnects, and their power consumptions will be the same under the same conditions, their energy consumptions are excluded from the calculation of total energy consumptions. Energy consumptions of both interconnects are shown on the chart from 0 to 8 pJ/bit. By definition, high efficiency interconnect consumes less power, and its value of energy consumption is small. On the other hand, low-efficiency interconnect has a large value of energy consumption.

As shown in Fig. 16, the energy consumption of interchip electrical interconnects has obvious frequency and interconnect length thresholds. For example, if the frequency is 30 GHz, the threshold interconnect length is 29 cm. If the interconnect length is 50 cm, the threshold frequency is 12 GHz. When the frequency and the interconnect length are smaller than thresholds, the energy consumption is <1 pJ/bit. When the frequency or the interconnect length exceed the thresholds, the energy consumption will rapidly be increased to infinity. As shown in Fig. 17, the energy consumption of interchip optical interconnects is increased gradually without obvious thresholds, compared with that of interchip electrical interconnects. At large working frequency or interconnect length, the value of energy consumption is still comparable with the energy efficiency of the whole system. For example, at 60-GHz working frequency and 100-cm interconnect length, the energy consumption of optical interconnects is 7.9 pJ/bit. This value is about an order of magnitude larger than the energy consumption of optical interconnects when the frequency and the interconnect length are small.

D. Bandwidth Density

The bandwidth densities of electrical interconnects and optical interconnects are plotted in Fig. 18 showing area bandwidth densities, and in Fig. 19 showing linear bandwidth densities. For electrical interconnects, two typical of packages are studied: 1) the Fineline BGA package and 2) the Micro Fineline BGA package [34]. The distance between two neighboring differential pairs is assumed to be 48 mil (1.21 mm) as the normal pitches, and 24 mil (0.61 mm) as the dense pitches. For optical interconnects, the area bandwidth densities and the linear bandwidth densities are calculated based on an IBM prototype [4]. It shows that both the area and the linear bandwidth densities of the optical interconnects are at least one order of magnitude larger than those of electrical interconnects. The area and the linear bandwidth densities of the WDM-based optical interconnects are either about two orders of magnitude larger than those of electrical interconnects with the Micro FBGA package or the dense pitches. The optical interconnects show the advantages of bandwidth densities over electrical interconnects. The number of signal pins on the package or the number of layers in the PCB board can effectively be reduced.

With the development of technology, demand for the number of pins is growing [44]. However, the maximum pin count is limited by physical constraints of chip package, and could not be increased dramatically. The total number of pins on the chip package can effectively be reduced by replacing some of the electrical interconnects with the optical interconnects. The pin count comparison is shown in Fig. 20. According to the ITRS report [44], about half of pins are for signals and the rest half of pins are for power and ground.
The estimations of pin count under different technologies are collected from the ITRS report. It shows that by implementing optical interconnects instead of electrical interconnects, at least 92% signal pins can be reduced when connecting chips more than 25 cm (10 in) apart. For instance, the total number of pins under 8 nm technology is 2600. This value is slightly larger than the total number of pins under 24-nm technology before the replacement. In addition, if chips are connected more than 50 cm (20 in) apart, more than 97% signal pins are reduced. If the interconnect length is increased, the percentage of saved signals pins is increased.

**E. Latency**

The latency of electrical interconnects and optical interconnects are plotted in Fig. 21. For electrical interconnects, traces can be fabricated on traditional FR-4 board, or be fabricated on a different board with a lower value of dielectric constant, such as RO4003 board. For optical interconnects, chips can be connected by polymer waveguides on board [38], or connected by flexible single-mode fibers [22]. Cases when interconnect length are <100 cm are evaluated, which are the typical lengths of interchip interconnects. It shows that the relationship between the latency and the interconnect length is linear. Among those four types, the fiber-based optical interconnect has the smallest latency. Its latency is 27% less than that of traces on FR-4 board, and 23% less than that of traces on RO4003 board. The waveguide-based optical interconnect has the second smallest latency, which is 23% less than that of traces on FR-4 board, and 18% less than that of traces on RO4003 board. Compared with traditional electrical signals, it takes less time for optical signals to be transmitted from one chip to the other. Hence, optical interconnects are better choices in terms of latencies.

**VII. Conclusion**

Energy consumptions, bandwidth densities, and latencies are analyzed and compared between two types of interchip interconnects: 1) low-swing differential electrical interconnects and 2) polymer waveguide-based optical interconnects. First, the energy consumption of optical interconnect is comparable with that of electrical interconnect if the transmission bandwidth or the interconnect length is less than threshold points. On the other hand, it will be nearly 100% less than that of electrical interconnect if the transmission bandwidth or the interconnect length is greater than threshold points. Second, the area bandwidth density and the linear bandwidth density of optical interconnects are at least one order of magnitude larger than those of electrical interconnects. When the interconnect length is increased, the differences are further increased. Therefore, optical interconnects can significantly reduce I/O pin count. For example, the I/O pin count can be reduced by at least 92% when connecting chips more than 25 cm (10 in) apart, and at least 97% when connecting chips more than 50 cm (20 in) apart. Finally, the latency of fiber-based optical interconnects is 27% less than that of electrical interconnects, and the latency of waveguide-based optical interconnects is 23% less than that of electrical interconnects. In conclusion, optical interconnects have lower power consumption, higher bandwidth density, and smaller latency than electrical interconnects. They could effectively improve chip pin performance and alleviate chip pin constraints for manycore processors. They could be implemented as potential alternatives for electrical interconnects in the near future.

**ACKNOWLEDGMENT**

The authors would like to thank Prof. A. Poon and Y. Zhang from The Hong Kong University of Science and Technology, Hong Kong, for their useful and constructive discussions on this work.

**REFERENCES**

[1] PCI Express 4.0 Evolution to 16 GT/s, Twice the Throughput of PCI Express 5.0 Technology, PCI-SIG, Beaverton, OR, USA, 2011.


[32] W. Hofmann, M. Müller, G. Bohn, M. Ortsiefer, and M.-C. Amann, “1.55 μm InP-based VCSEL with enhanced modulation bandwidths $\geq 10$ GHz up to 85 $^\circ$C,” in Proc. OFC, Mar. 2009, pp. 1–3.


[34] Designing With High-Density BGA Packages for Altera Devices, Altera Corp., San Jose, CA, USA, 2014.


Xuan Wang (S’12) received the B.S. degree in electronics engineering from Shanghai Jiao Tong University, Shanghai, China, in 2009. He is currently pursuing the Ph.D. degree in electronic and computer engineering with The Hong Kong University of Science and Technology, Hong Kong.

Zhifei Wang (S’15) received the B.S. degree in electronics engineering from Zhejiang University, Hangzhou, China, in 2014. He is currently pursuing the Ph.D. degree in electronic and computer engineering with The Hong Kong University of Science and Technology, Hong Kong.

Zhe Wang (S’14) received the B.S. degree in electronics engineering from Shanghai Jiao Tong University, Shanghai, China, in 2011. He is currently pursuing the Ph.D. degree in electronic and computer engineering with The Hong Kong University of Science and Technology, Hong Kong.

Rafael Kioji Vivas Maeda (S’15) received the B.S. degree in electrical engineering from the Federal University of Minas Gerais, Belo Horizonte, Brazil, in 2013. He is currently pursuing the Ph.D. degree in electronic and computer engineering with The Hong Kong University of Science and Technology, Hong Kong.

Luan Huu Kinh Duong (S’14) received the B.S. degree in computer science from The Hong Kong University of Science and Technology, Hong Kong, in 2012, where he is currently pursuing the Ph.D. degree in electronic and computer engineering.

Haoran Li (S’15) received the B.S. degree in electronics engineering from Zhejiang University, Hangzhou, China, in 2014. He is currently pursuing the Ph.D. degree in electronic and computer engineering with The Hong Kong University of Science and Technology, Hong Kong.