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Patterned p-Doping of InAs Nanowires by Gas-Phase Surface Diffusion of Zn

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ABSTRACT Gas phase p-doping of InAs nanowires with Zn atoms is demonstrated as an effective route for enabling postgrowth dopant profiling of nanostructures. The versatility of the approach is demonstrated by the fabrication of high-performance gated diodes and p-MOSFETs. High Zn concentrations with electrically active content of $\sim 1 \times 10^{19}$ cm^{-3} are achieved which is essential for compensating the electron-rich surface layers of InAs to enable heavily p-doped structures. This work could have important practical implications for the fabrication of planar and nonplanar devices based on InAs and other III−V nanostructures which are not compatible with conventional ion implantation processes that often cause severe lattice damage with local stoichiometry imbalance.

KEYWORDS Nanoscale doping, p-type MOSFETs, diodes, III−V nanowires, zinc dopants

In the endless trend to shrink transistor dimensions to increase density and performance, planar devices are reaching the threshold for many desirable device characteristics.[1] To this end, many other novel transistor structures are being explored. In particular, much research has been devoted to transistors with nanowire (NW) channels due to their excellent electrostatic properties.[2,3] One very promising semiconductor for NW devices is InAs, due to its excellent electron mobilities,[4−6] and ease of nanoscale, metal Ohmic contact formation to the conduction band via solid source reactions.[7] However, there remain many challenges to be addressed with InAs NW device fabrication. Specifically, one fabrication issue that requires attention is the dopant profiling of InAs NWs. p-type doping of InAs NWs is particularly challenging given the surface electron-rich layer that causes the surface Fermi level to be pinned in the conduction band for an undoped NW. Although techniques such as in situ doping during the growth have been previously reported for NWs,[8−10] postgrowth patterned doping is desired for most device fabrication schemes. Notably, conventional ion-implantation techniques are not compatible with nanoscale InAs semiconductors due to the severe crystal damage induced during the implantation process resulting in In atom clustering which cannot be fixed by a subsequent annealing process. In that regard, surface doping processes are highly attractive.[11−13] To address this need, here, we report patterned p-doping of InAs NWs with Zn atoms by using a postgrowth, surface doping approach. The versatility of the approach is demonstrated by configuring the doped NWs into various device structures, including p$^+$−n diodes, and p-MOSFETs.

InAs NWs used in this work were grown using the vapor−liquid−solid (VLS) method by chemical vapor deposition in a two-zone tube furnace using solid InAs powder source. As previously described, a 0.5 nm thick Ni film was annealed at 800 °C for 10 min to create nanoparticles that serve as catalysts.[14] A substrate temperature of 490 °C, source temperature of 720 °C, and pressure of 5 Torr with H_2 carrier gas (200 SCCM flow rate) were used. The grown NWs were harvested by sonication in anhydrous ethanol and dropcasted on Si substrates. To p-dope the NWs with Zn atoms, the samples were placed in a tube furnace with solid Zn powder used as the source. The NW substrate and Zn source were placed ~6 cm apart with the furnace temperature set at 400−415 °C for 1 min (as counted from temperature stabilization time). A chamber pressure of 650 Torr with Ar atmosphere was used. To achieve patterned doping, a SiO_2 mask was deposited to partially cover the NWs on substrates. The diffusion length of Zn atoms can be approximated as $2(Dt)^{1/2}$, where D is the diffusion coefficient and t is the diffusion time. A diffusion coefficient $D \sim 1.4 \times 10^{-12}$ cm^2/s at 400 °C for Zn in InAs bulk substrates is reported in the literature.[15] Given this diffusion coefficient value, a diffusion length of ~180 nm is estimated for $t = 1$ min used in our experiments. This indicates that under our process conditions, InAs NWs are fully doped across their diameter (i.e., $d <$ diffusion length), but that Zn atoms are unable to diffuse far along the length of the NW or underneath the SiO_2 mask once incorporated into the NW. This is an important requirement for the fabrication of p−n junctions. This diffusion length is relatively small given that our devices are long channel devices with channel lengths of $L = 6-10$ μm. In the future, shorter annealing times can be

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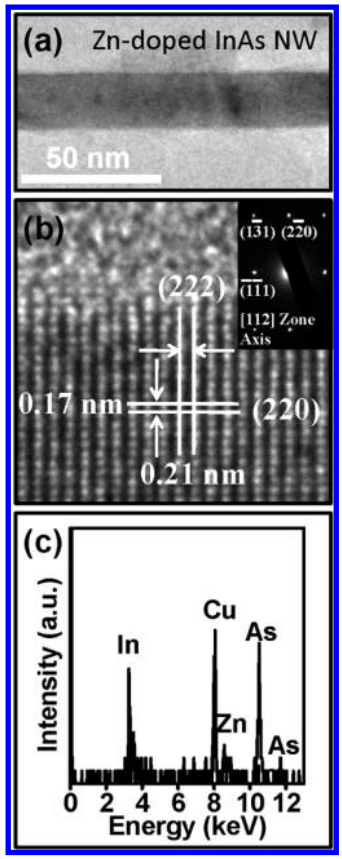

FIGURE 1. (a) Low-resolution and (b) high-resolution TEM images of a Zn-doped InAs NW with diffraction pattern shown in the inset. (c) EDS analysis of a Zn-doped InAs NW, depicting an elemental composition of ~5 atom % Zn.

explored to further reduce the diffusion length, as needed for short channel devices.[12] It should be noted that the diffusion parameters used for this analysis are for the bulk substrates as there are no values reported for the NW system. In the future, detailed studies of dopant diffusion in various NW systems are needed to enable more accurate understanding of the process.

Low-resolution and high-resolution transmission electron microscopy (TEM) images of a Zn-doped InAs NW are shown in panels a and b of Figure 1. The high-resolution TEM image shows the single-crystalline and defect-free nature of the doped InAs NW for which two planes, (222) and (220), are indexed. The diffraction pattern is shown in the inset with a [112] zone axis. Figure 1c shows the energy dispersion spectroscopy (EDS) quantitative analysis of a Zn-doped InAs NW for which the elemental composition of ~5 atom % Zn can be identified. Given the atomic density of 1.8×10^{22} cm^{-3} for InAs, this corresponds to a Zn concentration of [Zn] $\sim 9 \times 10^{20}$ cm^{-3}. It should be noted that this concentration is over an order of magnitude higher than the [Zn] $\sim 3 \times 10^{19}$ cm^{-3} reported in the literature for bulk InAs using a diffusion temperature of 500 °C.[15] This may be the result of a fraction of the Zn atoms remaining on the surface of the NWs or that the NW system exhibits a higher solid solubility limit as compared to the bulk.

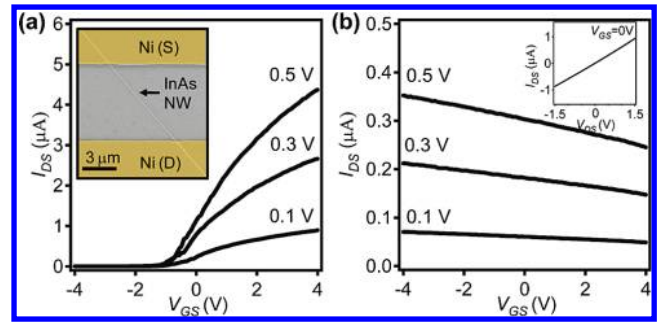

FIGURE 2. The $I_{DS}-V_{GS}$ characteristics of a representative (a) as-grown InAs NW with false-color SEM image of a representative device shown in the inset and (b) blank (i.e., unpatterned) Zn-doped InAs NW with $I_{DS}-V_{DS}$ plot for $V_{GS} = 0$ shown in inset. The heavily doped Si substrate is used as the global back gate with a gate dielectric thickness of 50 nm SiO_2.

To characterize the electrically active content of Zn dopant atoms, various device structures were fabricated and tested. In one case, back-gated devices were fabricated by photolithography on the dropcasted NW substrates (p^+Si/50 nm SiO_2) to define source (S) and drain (D). Ni was then thermally evaporated into the S/D regions to form contacts. The inset in Figure 2a shows a representative scanning electron microscope (SEM) image of such a back-gated NW device. Long channel lengths, $L = 6-10$ μm, are used to make sure that transport of carriers is in the diffusive, as opposed to ballistic or quasi-ballistic, regime. This enables the extraction of intrinsic transport properties, such as carrier mobility. The $I-V$ characteristics of a representative as-grown InAs NW and blank (i.e., unpatterned) Zn-doped InAs NW are shown in Figure 2. The as-grown InAs NW is n-type due to the high electron concentration that results from surface fixed charges and local imbalances in stoichiometry.[16] As previously discussed, there is a linear dependence of the device resistance on channel length, establishing that the Ni source/drain contacts to the conduction band of as-grown InAs NWs are Ohmic.[7] The as-grown NW exhibits an ON current of ~4.4 μA at $V_{DS} = 0.5$ V, $I_{ON}/I_{OFF} > 10^4$, and field-effect mobility of 4400 $cm^2/(V\ s)$ for channel length $L = 8$ μm and NW diameter $d = 27$ nm, consistent with the previously published observation.[16] The doped InAs NWs using the described process conditions are p^+ due to heavy Zn doping, exhibiting an ON current of ~0.4 μA at $V_{DS} = 0.5$ V with minimal gate dependence (Figure 2b). The linear behavior of the $I_{DS}-V_{DS}$ plot (Figure 2b inset) confirms that the contacts to the p^+ NW are near Ohmic. This is primarily due to the thinning of the Schottky barriers at the contacts to the valence band of NWs arising from the heavy Zn doping. From the $I_{DS}-V_{GS}$ characteristics, a hole field-effect mobility of ~30 $cm^2/(V\ s)$ for a NW diameter of $d \sim 30$ nm is estimated. This field-effect mobility is reasonable given that the hole Hall mobility of bulk InAs substrates for a doping concentration of $\sim 1 \times 10^{19}$ cm^{-3} acceptors is ~100

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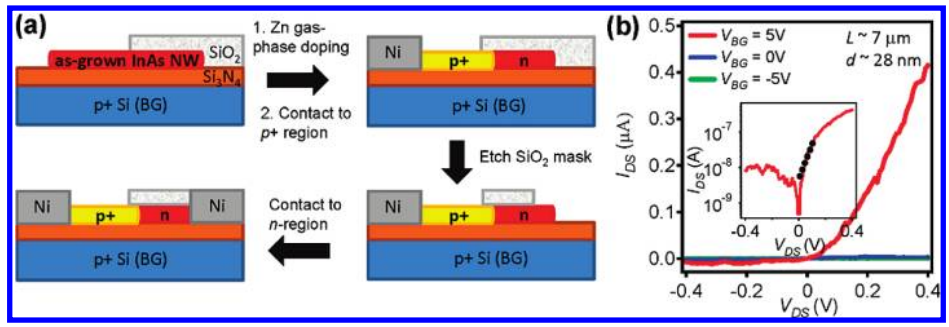

FIGURE 3. (a) The process flow for the fabrication of back-gated InAs NW diodes. (b)The $I-V$ behavior of a representative diode as a function of the back-gate voltage, V_{BG}. The inset shows the log scale plot for $V_{BG} = 5$ V and the fit to the ideal diode equation indicated by the dotted line.

$cm^2/(V\ s)$ at room temperature and that the measured Hall mobility is always larger than the extracted field-effect mobility.[17,18] Using the conductance $G \sim 6 \times 10^{-7}$ S and $d \sim 30$ nm, the resistivity, $\rho \sim 0.02\ \Omega$ cm, is estimated for the doped NW. From ρ and μ, the electrically active [Zn] is estimated to be $\sim 1 \times 10^{19}\ cm^{-3}$. This high electrically active [Zn] corresponds to degenerate doping, with the Fermi level E_F located ~0.024 eV below the valence band edge E_v. This electrically active Zn concentration is consistent with those reported for various dopants in bulk InAs substrates.[19,20] While most (~70%) NWs exhibited p^+ behavior (minimal gate dependence) for doping temperatures of >400 °C, some (~30%) NWs exhibited lightly p-type or ambipolar behavior. For doping temperatures <400 °C, roughly half of the NWs were ambipolar while the other half remained n-type. For the p^+ NWs, there was sufficient Zn doping to fully compensate the high intrinsic electron concentration, especially at the surface. However, for the ambipolar NWs, it is likely that the core of the NW is doped p-type while the high surface electron concentration "shell" remains n-type. This observation is especially expected for lower diffusion temperatures which effectively lowers the diffusion rate and the solid solubility limit of Zn.

For comparison, InAs NWs were also doped using Zn-ion implantation. Ion implantation energy of ~35 keV with dopant areal dose of 3.5×10^{12} to $3.5 \times 10^{13}\ cm^{-2}$ were used, followed by thermal annealing at 375 °C for 30 min. Scanning electron microscopy (SEM) clearly indicates that the NW surfaces are severely damaged by the ion implantation, and in some cases, the NWs were even broken with damage being the most apparent for the highest dopant dose of $\sim 3.5 \times 10^{13}\ cm^{-2}$ (see Figure S1 in Supporting Information). Furthermore, back-gated devices fabricated from the Zn-ion-implanted InAs NWs remained n-type with degraded ON currents and did not turn off, even after thermal annealing (see Figure S2 in Supporting Information), suggesting that the incorporated dopants are not electrically active and that the damage to the NW lattice degraded the electrical properties and enhanced the leakage currents. The failure of the Zn-ion-implantation approach to produce defect-free p-type NWs highlights the importance of the Zn surface doping scheme presented in this work for compound semiconductor nanostructures.

In order to show the versatility of the presented doping approach, various NW device structures involving dopant profiling were fabricated and tested. In one example, back-gated diodes were fabricated by patterned Zn doping of InAs NWs. The process flow is shown in Figure 3a. First, 60 nm of Si_3N_4 was grown by PECVD on p^+ Si substrates. As-grown InAs NWs were then dropcasted on the nitride substrate, and 70 nm electron-beam evaporated SiO_2 was deposited on photolithographically patterned regions to cover parts of the NWs, followed by lift-off of the resist. In this case, the evaporated SiO_2 served as the diffusion mask during the doping process. The NW substrates were then Zn-doped by the gas-phase surface doping process, with only the unmasked segments of the NWs exposed to Zn dopants. Ni contacts were then made to the Zn-doped segments of the NWs by photolithography and thermal evaporation. A final photolithography step, followed by etching in 50:1 HF to remove the SiO_2 mask and a subsequent Ni thermal evaporation were applied to contact the undoped regions (i.e., as-grown, n-type) of the NWs. The $I-V$ behavior of a representative diode is shown in Figure 3b. Here, $L \sim 7\ \mu$m and $d \sim 28$ nm. A rectifying behavior is observed for $V_{BG} > 0$. On the other hand, the device is insulating for $V_{BG} \leq 0$. This, along with the $I_{DS}-V_{GS}$ curves of Figure 2, indicates that the Zn-doped region of the NW is in fact p^+ and is always in the hole accumulation mode, while the n-type region is being modulated by the back-gate. The n-type segment becomes fully depleted for $V_{BG} \leq 0$, but turns to the accumulation mode for $V_{BG} > 0$ and $V_{DS} > 0$. The ideality factor of the p^+-n diode shown in Figure 3b is ~1.5, with the fit to the ideal diode equation indicated by the dotted line in the log scale inset. Notably, the process is also compatible with bulk InAs substrates with the NW and bulk diodes fabricated using the same approach, exhibiting similar properties (see Figure S3 in Supporting Information).

Next, back-gated InAs NW p-MOSFETs were fabricated utilizing the gas phase Zn doping to define the p^+ S/D contacts, with a schematic of the process shown in Figure 4a. Briefly, undoped InAs NWs were dropcasted on p^+Si/SiO_2

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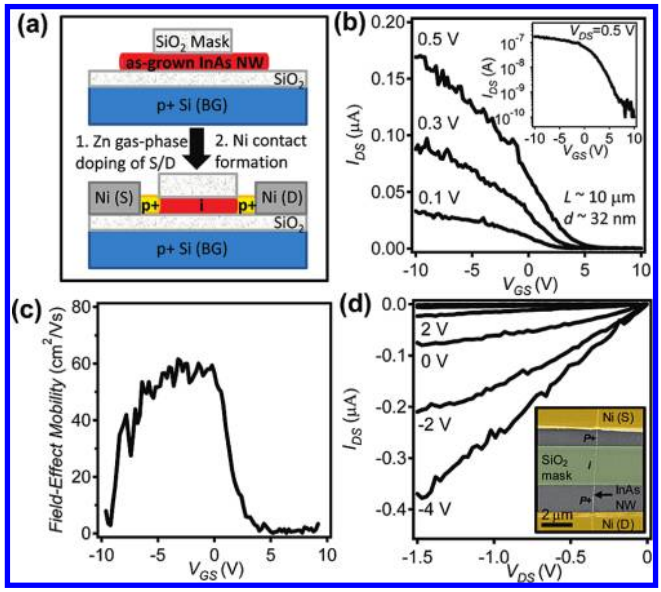

FIGURE 4. (a) A schematic of the back-gated InAs NW p-MOSFETs. (b) The $I_{DS}-V_{GS}$ behavior of a representative p-MOSFET with the log scale plot shown in the inset. (c) Hole field-effect mobility of the device as a function of the back-gate voltage. (d) The output characteristics of the same NW p-MOSFET with false-color SEM image of a representative p-MOSFET shown in inset.

(50 nm thermally grown) substrates and photolithography was used to pattern SiO_2 (~70 nm thick) mask regions on top of the NWs. NW substrates were then Zn-doped as previously described. The exposed nanowire ends were made p^+ while the NW segment under the SiO_2 mask remained undoped. Photolithography and thermal evaporation were then employed to form the Ni contacts on the p^+ S/D regions. The heavily doped Si substrate was used as the global back gate with a gate dielectric thickness of ~50 nm SiO_2.

The $I-V$ characteristics of a representative InAs NW p-MOSFET is shown in parts b and d of Figure 4, with an SEM image of a representative device as the inset in Figure 4d. The p-MOSFET has $I_{ON} \sim 0.17$ μA and $I_{OFF} \sim 0.1$ nA at $V_{DS} = 0.5$ V, with an $I_{ON}/I_{OFF} > 10^3$. The threshold voltage V_t is shifted to a positive voltage, likely as a result of fixed oxide and interface trapped charge states at the interface of the NW n-segment and the evaporated SiO_2 mask. The field-effect mobility as a function of V_{GS} is shown in Figure 4c, with a peak hole mobility of ~60 $cm^2/(V\,s)$. The hole mobility for InAs NWs is significantly lower than the electron mobility as expected. This mobility is ~9 times lower than the Hall mobility of ~450 $cm^2/(V\,s)$ reported for lightly doped, p-type InAs bulk substrates.[21] The difference may be due to surface scattering and contact resistance associated with the field-effect mobility extractions. The $I-V$ behavior of the patterned Zn-doped p-MOSFET is in distinct contrast to the behavior of the blank Zn-doped NW device shown in Figure 2b which exhibits minimal gate dependence. Furthermore, in contrast to the blank-doped p^+ NW devices where the entire doped NW serves as the "channel" material, the p-MOSFET exhibits a higher hole mobility (~2 times higher) since the channel is undoped resulting in minimal impurity scattering.

In conclusion, we have demonstrated an equilibrium-based method to heavily p-dope InAs NWs by gas-phase surface diffusion of Zn. Blank Zn-doped InAs NW devices exhibit minimal gate dependence, with a high electrically active dopant concentration of $\sim 1 \times 10^{19}$ cm^{-3}. By use of a patterned doping scheme, diodes with ideality factors of ~1.5 are fabricated with electrical characteristics confirming one-sided junction formation arising from the heavily Zn-doped regions. Finally, InAs NW p-MOSFETs with $I_{ON}/I_{OFF} > 10^3$ and hole field-effect mobility $\mu \sim 60$ $cm^2/(V\,s)$ are achieved, demonstrating the effectiveness of our patterned doping technique. While InAs p-MOSFETs are not ideal devices due to the low hole mobility of InAs, this work shows the versatility and the effectiveness of the presented doping approach for fabrication of complex device structures. This process scheme is highly promising for the future fabrication of high-speed diodes and low power tunneling field-effect transistors based on InAs nanostructures which are not compatible with conventional ion implantation processes.

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Supporting Information Available. SEM images and electrical characteristics of Zn ion-implanted InAs NWs used as controlled experiments and the bulk InAs diodes fabricated by the gas-phase surface diffusion of Zn. These materials are available free of charge via the Internet at http://pubs.acs.org.

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