

## *In situ* doping control and electrical transport investigation of single and arrayed CdS nanopillars†

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Highly aligned intrinsic and indium doped CdS nanopillar arrays were fabricated *via* a template assisted Solid Source Chemical Vapor Deposition method (SSCVD). The prepared nanopillar arrays were well aligned, dense and uniform in diameter and length. Their geometry can be well defined by the design of the templates. These unique properties make them promising candidates for future photonic and optoelectronic devices. The structure of the prepared nanopillars has been studied by high resolution transmission electron microscopy and their different growth orientation as compared to those grown in free space has been observed and interpreted by the template induced change of the liquid–solid interfacial energy and the surface tension at the edge of the circular interface. To investigate electrical property of CdS nanopillars, vertical nanopillar array devices and horizontal individual nanopillar field-effect transistors have been fabricated and characterized. The measurements showed that the location of the indium doping source significantly affected carrier concentration, conductivity and field-effect mobility of the prepared CdS nanopillars. Particularly, it was found that conductivity could be improved by 4 orders of magnitude and field-effect mobility could be enhanced up to  $50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  *via* proper doping control. These results enable further applications of CdS nanopillars in nano-optoelectronic applications such as photodetection and photovoltaics in the future.

### 1 Introduction

Compound semiconductor nanowires (NWs) with a wide range of choice of energy band-gaps have been extensively explored as

building blocks for nanoscale electronic devices such as field-effect transistors (FETs),<sup>1–6</sup> electronic devices such as solar cells,<sup>7–9</sup> light emitting diodes,<sup>10,11</sup> and lasers.<sup>12,13</sup> Apart from their advantageous small dimensions for device miniaturization, semiconductor NWs have shown intriguing properties that promise high device performance. For example, semiconductor NWs have shown impressively high gain and quantum efficiency for photodetection due to high density of surface states,<sup>14,15</sup> and optical confinement of photons inside NW cavities leads to lowering of lasing threshold.<sup>16,17</sup> Among all the compound semiconductor NWs, CdS NWs have attracted increasing attention for applications including plasmonic lasers,<sup>18</sup> solar cells,<sup>19,20</sup> photodetectors<sup>21,22</sup> and laser cooling devices<sup>23</sup> demonstrated recently. In these applications the geometry of the CdS NWs needs to be precisely controlled, particularly for laser application which utilizes NWs as Fabry–Perot resonators. Meanwhile, the tunability of electrical properties of CdS NWs, including doping level and carrier mobility, is also essential for implementing high-performance optoelectronic devices. However, the conventional bottom-up growth of CdS NWs in free space using a catalytic process lacks precise control over NW length and diameter, and, especially, controllable *in situ* doping of CdS NWs has rarely been reported. In this work, catalytic growth of CdS NWs has been confined inside well-defined nanochannels in anodic alumina membranes (AAMs). Meanwhile, *in situ* doping using metallic indium (In) as the dopant source was performed. It was found that due to the precise control of nanochannel length and diameter in AAMs, CdS NWs have quite uniform length and diameter distribution with a small standard deviation. As compared with post-doping and annealing, the *in situ* doping approach used in this work is a more convenient approach to achieve nanowire growth and doping in one step. Meanwhile, due to the fact that the dopant atoms were incorporated during growth, the distribution of the dopant is expected to be uniform. In order to characterize electrical properties of CdS NWs, both vertical NW array devices and single NW field-effect transistors (FETs) have been fabricated. Electrical measurements showed that Indium doping in

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CdS NWs significantly increased their conductivity and carrier concentration, as well as field-effect mobility. These results can be further harnessed to implement CdS NW-based nano-optoelectronic devices with optimized performances.

## 2 Experiments

The nanopillar growth template AAMs were prepared through a two-step anodization of high-purity aluminum foils reported previously.<sup>24</sup> Briefly, the aluminum chip was first electro-polished in an acidic solution (25 vol% HClO<sub>4</sub> mixed with 75 vol% absolute CH<sub>3</sub>CH<sub>2</sub>OH) under a 10 V direct current (DC) voltage for 2 min and then anodized in a 0.3 M oxalic acid aqueous solution for 3 h using a DC voltage of 60 V. The porous Al<sub>2</sub>O<sub>3</sub> layer from this anodization step was etched away by a mixture solution (6 wt% H<sub>3</sub>PO<sub>4</sub> and 1.8 wt% CrO<sub>3</sub>) at 70 °C for 30 min, followed by a second anodization process in the same oxalic acid aqueous solution for 42 min. Note that in this process the length of the nanochannels was controlled by the AAM second anodization time and the growth rate, which is 125 nm min<sup>-1</sup> in our case. After the second anodization, the template was further etched in a H<sub>3</sub>PO<sub>4</sub> aqueous solution (5 wt%, 52 °C) for 8 min to widen the channels to 130–140 nm. Afterwards, a current ramping process was carried out to thin down the barrier layer at the bottom of the AAM channel to several nanometers, followed by the electrodeposition of a Au catalyst with a commercial electroplating solution (Gold ES 25 RTU Elevate 7990, Techni Gold) of 200–300 nm length at the barrier layer thinned position.<sup>24,25</sup>

The CdS nanopillar growth with the prepared AAM templates was carried out in a 1-inch horizontal quartz tube furnace (OTF 1200X-II, MTI) with two resistive heating zones *via* a solid source chemical vapor deposition method as shown schematically in Fig. 1a and b. 1 g CdS powder (99.999%, China Rare Metal) was firstly put inside a secondary quartz tube with 20 cm length and 1 cm diameter as the source. Then the secondary tube was placed inside the 1-inch furnace tube on the up flow; thus the CdS powder was 4.5 cm away from the middle point of the furnace (location O in Fig. 1a), indicated as location A in Fig. 1a. Meanwhile, an AAM sample was placed

inside a quartz vial with 0.9 cm inner diameter, and the vial was put on the left end of the secondary quartz tube with ~5 mm internal overlap, as shown in Fig. 1a. As a result, the growth substrate was placed in location D, which is 10 cm away from the middle of the furnace, location O. It is worth pointing out that this configuration has never been reported before. The function of the secondary quartz tube together with the sample vial is to maintain the high source vapor pressure inside to improve the efficiency of the growth, as well as to reduce CdS deposition on the furnace tube. During the growth, 100 sccm H<sub>2</sub> gas was kept flowing in the CVD system and the system pressure was stabilized at 12 torr. The left and right zone temperatures were set as 580 °C and 700 °C, respectively. However, due to the internal temperature gradient (Fig. S1†) and the fact that the CdS source was not in the middle of the right zone, the actual source temperature was 682.4 °C. After 20 min growth, the furnace was turned off and cooled to room temperature naturally. Then the yellowish product was found on the AAM only in the region where the Au catalyst was electrochemically deposited indicating catalyzed material growth. Note that the past study has shown that intrinsic CdS, either bulk or nanostructures, showed poor conductivity,<sup>26</sup> which is not desirable for device applications. In order to improve conductivity of CdS, many elements, such as Sn,<sup>27</sup> Ga<sup>28</sup> and Mn,<sup>29</sup> have been used to dope CdS. In this work, indium was chosen as the dopant as it is already proved to be an effective dopant to tailor the electrical and optical properties of CdS films.<sup>30,31</sup> Specifically, *in situ* indium doping was conducted with 80 mg of indium metal pellets. As shown in Fig. 1a, the doping level can be controlled by placing indium pellets at different positions, corresponding to different indium evaporation temperature and source–substrate distance.

In this work, three kinds of samples were prepared: undoped CdS nanopillars and the nanopillars doped with the indium source at locations B and C. Therefore, these three types of samples are labeled as samples U, B and C, respectively. In fact, location B is 24 cm away from location D where the growth substrate was placed, and the actual temperature at location B is 692 °C measured with an external thermocouple. And location C is 32 cm away from location D with an actual temperature of 601 °C. After CdS growth, the top surface of the prepared sample was cleaned by ion milling (Gantan 691) with a ~1.5° beam incident angle for 40 min. Then the sample was flipped over and glued to a glass substrate by epoxy, followed by etching away of the Al foil with a saturated HgCl<sub>2</sub> solution and a second ion milling (5° angle for 20 min) to remove the thin subchannels at the backside. Eventually, the CdS nanopillars will be released from the AAM template by completely dissolving Al<sub>2</sub>O<sub>3</sub> in 1 M NaOH. Thereafter, photoluminescence (PL) spectra (measured on a bulk-photoluminescence setup with 28 mW of a He–Cd CW laser (325 nm)) of the obtained free standing CdS nanopillars have been obtained for the doped (samples B and C) and undoped (sample U) samples. The nanopillars have also been dispersed into isopropyl alcohol by ultra-sonication for high-resolution transmission (HRTEM) characterization and single nanopillar FET device fabrication.

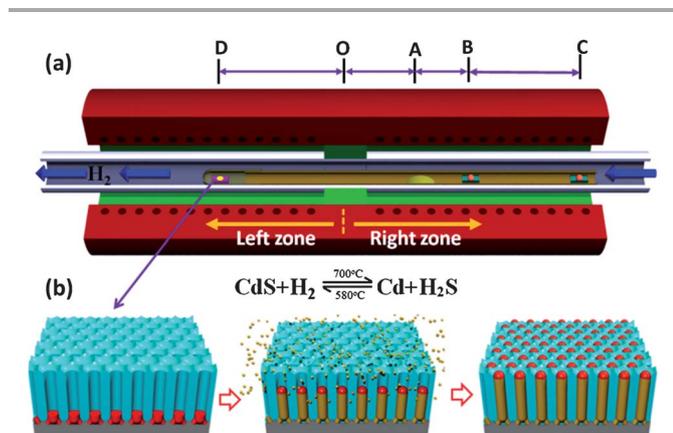


Fig. 1 Schematic representation of the CVD setup and the growth process.

### 3 Results and discussion

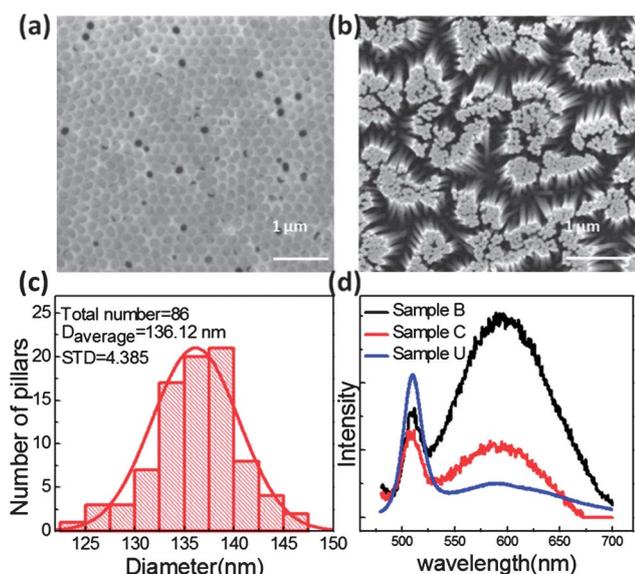
#### 3.1 Material characterizations

Nano-engineered AAMs have been widely used for integration of quasi-one-dimensional materials and templates for light harvesting structures.<sup>32–34</sup> Catalytic growth of ZnO NWs in confined channels has been shown to follow a vapor–liquid–solid process in which liquid metal nanoparticles are kept on top of the NWs during growth.<sup>24</sup> In order to confirm that CdS nanopillar growth follows the same process, a cross-sectional back-scatter electron (BSE) microscopic image was obtained on a CdS nanopillar grown in a 2  $\mu\text{m}$  thick AAM with a pore size of  $\sim 250$  nm for ease of observation. As shown in Fig. S2,<sup>†</sup> due to precise control of CdS growth time, most of the CdS nanopillars just grew up to the upper surface of the AAM, and Au nanoparticles can be clearly resolved on top of nanopillars. In reality, such a precise growth time control is rather challenging; therefore prolonged growth is typically performed to make sure that CdS nanopillars have grown out of the channels. In order to remove extra CdS nanopillars outside AAM channels, long angle and short time ion milling was performed on samples. After ion milling, a CdS nanopillar filling condition can be clearly observed, as shown in Fig. 2a, demonstrating a high packing density of  $\sim 10^{11}$   $\text{cm}^{-2}$  and  $\sim 97\%$  typical channel filling ratio. In order to obtain free standing CdS nanopillars, the AAM was transferred to a glass slide with epoxy glue, followed by fully etching away  $\text{Al}_2\text{O}_3$  in 1 M NaOH (Fig. S3<sup>†</sup>). Fig. 2b shows high density free standing CdS nanopillars after being released from the AAM and it can be seen that the nanopillars have not only uniform length, but also very small diameter variation. This observation can be further confirmed with a histogram of nanopillar diameter statistics as shown in Fig. 2c, demonstrating an average nanopillar diameter

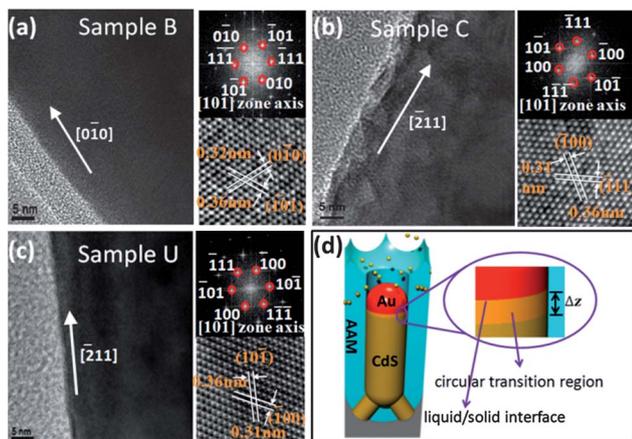
of 136.12 nm with only 4.39 nm standard deviation. As a comparison, CVD growth of CdS NWs has also been performed on a planar Si substrate decorated with 50 nm Au nanoparticles as catalysts under the same growth conditions. However, as is apparent in Fig. S4,<sup>†</sup> due to the un-controlled free growth, CdS NWs have large variation in diameter and length with poor density. This fact clearly shows the advantage of template growth of semiconductor NWs/nanopillars for precise geometry control.

To examine the optical quality of the grown CdS nanopillars, room temperature PL spectra for free standing nanopillar array samples labeled as B, C and U were obtained and are shown in Fig. 2d. It can be seen that all the spectra consist of a sharp emission band at 510 nm (2.43 eV) and a broad emission band centered at 596 nm (2.08 eV). The first band corresponds to the band-gap emission of the CdS and the second band can be attributed to the transition from Cd-interstitial donor states to the valence band edge.<sup>35,36</sup> The intensity of this band increases with that of the doping level but the position does not change. This can be explained as the result of more indium dopants substituting more Cd in the lattice leading to more Cd interstitials.<sup>37,38</sup> Interestingly, sample B shows dominant defect emission with sample C having comparable band-gap and defect emission intensity, whereas the undoped sample U shows dominant band-gap emission indicating high optical quality. This fact suggests that indium dopant incorporation accounts for defect emission in our work and sample B has a higher indium doping level than sample C.<sup>39</sup> In fact, as mentioned before, the indium source temperatures for samples B and C were 692  $^\circ\text{C}$  and 601  $^\circ\text{C}$ , respectively. The higher temperature at location B than location C results in much higher indium vapor pressure during *in situ* doping. In addition, location B is closer to growth location D compared with location C; therefore sample B demonstrated higher indium doping level and defect emission intensity.

To further characterize chemical composition and crystal structure of the prepared CdS nanopillars, they were drop-casted onto copper grids for TEM observation. Fig. S5 and S6<sup>†</sup> show low magnification TEM images of indium doped CdS nanopillars (samples B and C) capped with Au nanoparticles. It can be seen that the nanopillar surface is clean and smooth with uniform diameter. Energy-dispersive X-ray (EDX) spectroscopy images obtained at locations 1, 2 and 3 confirm that the cap is rich in Au and the nanopillar is composed of close to stoichiometric Cd and S with marginal indium composition within the EDX detection limit. Meanwhile, Fig. 3a–c demonstrate HRTEM images of samples B, C and U, respectively. The results revealed that all the samples are single crystalline with wurtzite structure. The undoped (sample U) and lightly doped (sample C) nanopillars show a growth direction of  $[211]$ , different from that of the CdS NW obtained with free growth which was reported as the  $[001]$  direction.<sup>40,41</sup> With the increasing doping level, the growth direction of the heavily doped samples (sample B) changed to  $[0\bar{1}0]$ . Since many of the material properties are orientation dependent, it is worthwhile exploring the mechanism of the change of the growth direction. Previous studies of VLS growth have shown that the NW growth



**Fig. 2** (a) Top view of nanopillar arrays embedded in the template. (b) Undoped CdS nanopillar arrays after removing the AAO template. (c) Statistical diameter distribution of the above nanopillars. (d) Room temperature PL analysis of CdS nanopillars with different doping levels.



**Fig. 3** Schematic of AAM template assisted VLS growth (a) and HRTEM (b–d) of CdS nanopillars with different doping levels.

direction is determined by formation of the lowest-free energy surfaces.<sup>42</sup> The energy close to the liquid–solid interface is particularly important as the NW growth occurs at this interface. The change of the growth direction can be triggered by change of the liquid catalyst alloy–solid NW interfacial energy ( $E_i$ ) and the energy associated with surface tension from the edge of the circular interface ( $E_s$ ).<sup>43,44</sup> The liquid catalyst–solid NW interfacial energy is determined by the interface area ( $A$ ) and liquid–solid surface tension ( $\sigma_{is}$ ). The surface tension energy from the edge of the circular interface ( $E_s$ ) is the product of the NW surface tension ( $\sigma_s$ ) and its effective area. The latter can be further expressed as the product of the circumference of the NW cross-section ( $L = \pi D$ , where  $D$  is diameter of the NW) and the thickness of the liquid–solid interfacial region on the NW side ( $\Delta z$ ). Thus, for a certain growth direction, the free energy of the interface can be eventually written as:<sup>43</sup>

$$F = E_s + E_i = \sigma_s \Delta z \pi D + \sigma_{is} A \quad (1)$$

Fig. 3d shows the schematic of AAM template guided VLS growth of a CdS nanopillar. Compared to the free growth of many II–VI NWs with a wurtzite structure, such as ZnO, CdS, CdSe, which usually have a preferential growth direction of [001] the growth direction of CdS nanopillars here changed to  $[\bar{2}11]$ . This change can be attributed to the fact that the nano-channel sidewall affects the surface tension of the NW ( $\sigma_s$ ) and  $E_s$ . Meanwhile, after heavy doping by indium, the growth direction further changed to  $[0\bar{1}0]$ . This can be explained as the formation of a Au–Cd–In ternary liquid phase leading to a different liquid–solid interface tension ( $\sigma_{is}$ ) and change of liquid–solid interfacial energy ( $E_i$ ).<sup>45</sup> In fact, it has been reported that indium doping can promote growth of ZnO NWs in the non-polar [110] direction but inhibit the [001] growth.<sup>46</sup> It may play a similar role as in CdS NW growth.

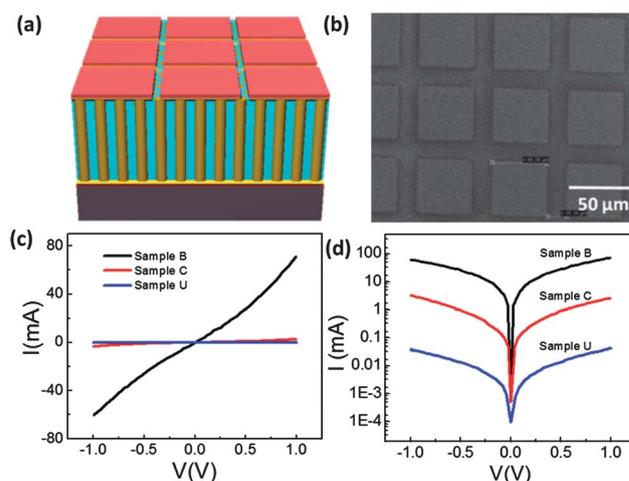
### 3.2 Electrical measurements

The electrical properties of undoped and indium-doped CdS nanopillars have been characterized *via* configuring a nanopillar

array into vertical devices as shown schematically in Fig. 4a. In this case a layer of a Ti/Au (10 nm/90 nm) metal film was deposited on top of an AAM with CdS nanopillars embedded inside when the entire sample was still on an Al supporting substrate (Fig. S3(a)†); then the AAM was transferred to a glass slide with epoxy glue followed by removing Al with saturated  $\text{HgCl}_2$  solution etching and bottom  $\text{Al}_2\text{O}_3$  barrier layer with an ion milling process. Then a copper TEM grid was used as a shadow mask to evaporate an array of Ti/Au (10 nm/90 nm) metal pads with dimensions of  $46 \mu\text{m} \times 46 \mu\text{m}$  area and  $16 \mu\text{m}$  space between two adjacent pads. The Ti/Au bilayer was chosen as the contact material because the relatively low work function of Ti (4.3 eV (ref. 47)) matches well with that of CdS (undoped CdS: 4.7 eV (ref. 48 and 49)), which will favor the formation of ohmic contact.<sup>50,51</sup> Note that in this experiment, the AAM template was anodized with 200 V DC voltage; thus the nanopillar diameter was  $\sim 220$  nm, pitch was 500 nm and the total number of nanopillars under each square metal pad was  $\sim 10\,000$ . The  $I$ – $V$  curves of samples B, C and U are shown in Fig. 4c, and the near linear curves indicate ohmic contacts with nanopillars. And the large difference in conductance for these three samples can be clearly observed. Fig. 4d demonstrates the same  $I$ – $V$  curves in a logarithmic scale. Specifically, doped samples B and C show 60.5 mA and 3.2 mA with 1 V bias, respectively, while the undoped sample (sample U) shows only  $\sim 38 \mu\text{A}$  current under same bias conditions. Furthermore, the conductivities of individual CdS nanopillars have been estimated using the following equation:

$$\sigma = \frac{L}{N\pi r^2 R} \quad (2)$$

where  $N = 10\,000$  is the number of CdS nanopillars under the electrode,  $L = 2 \mu\text{m}$  is nanopillar length,  $r = 110$  nm is nanopillar radius,  $R$  is resistance of the nanopillars. Therefore, the calculated conductivities for samples B, C and U are  $1.46 \text{ S cm}^{-1}$ ,  $4.61 \times 10^{-2} \text{ S cm}^{-1}$  and  $7.37 \times 10^{-4} \text{ S cm}^{-1}$ , respectively. These results clearly suggest that indium *in situ* doping in CdS nanopillars can improve their conductivity by four orders of magnitude in our work.



**Fig. 4** The schematic (a) and SEM (b) images of a CdS nanopillar array based device and its output characteristic curves in linear (c) and logarithmic (d) forms.

To further characterize electrical transport property of CdS nanopillars, they have also been fabricated into single nanopillar FETs using photolithography and subsequent metal deposition, as shown in Fig. 5a and b. In this case, 50 nm SiO<sub>2</sub> layer coated p-type (100) silicon chips were used as substrates to provide back-gate potential. The representative  $I_{ds}$ - $V_{ds}$  curves of samples B, C and U obtained at 0 V  $V_{gs}$  are displayed in Fig. 5c. Consistent with Fig. 4d, CdS nanopillar B demonstrates the highest conductance. Using eqn (2), the conductivities of single nanopillars grown under conditions B, C and U have been estimated as 1.42 S cm<sup>-1</sup>, 5.31 × 10<sup>-2</sup> S cm<sup>-1</sup> and 1.91 × 10<sup>-4</sup> S cm<sup>-1</sup>, respectively. These results agree well with those obtained from the vertical nanopillar array devices.

To evaluate carrier concentration and field-effect mobility of CdS nanopillars,  $I$ - $V_{gs}$  curves have been acquired for doping conditions B, C and undoped condition U, as shown in Fig. 5d-f. Overall, the n-type semiconducting behavior can be clearly identified from the fact that increasing gate potential results in increase of source-drain current. The nanopillar sample B demonstrates highest current with a gate threshold voltage of ~-14 V, while sample C shows a gate threshold voltage of ~-7.2 V. On the other hand, sample U demonstrates weak n-type behavior with unidentifiable gate threshold voltage without doping due to native S vacancy. The mobility and carrier concentration can be drawn from the following formulae:<sup>52</sup>

$$\mu_F = \left( \frac{dI}{dV_{gs}} \right) \times L \ln \left( \frac{2h}{r} \right) V_{ds} / (2\pi \epsilon_{SiO_2} \epsilon_0) \quad (3)$$

$$n = V_{gsth} / e \times 2\pi \epsilon_{SiO_2} \epsilon_0 / \ln \left( \frac{2h}{r} \right) \quad (4)$$

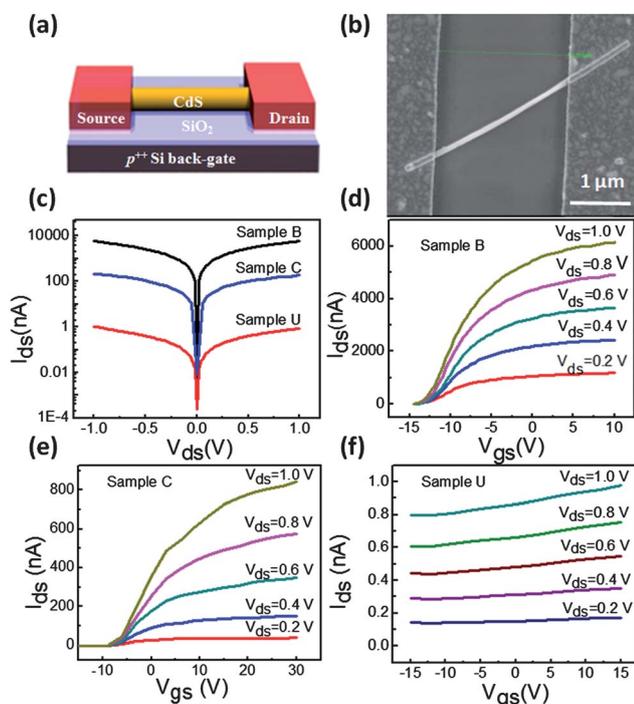


Fig. 5 The schematic (a) and SEM (b) images of single CdS pillar based FET devices and their output (c) and transfer (d-f) characteristic curves.

where  $dI/dV_{gs}$  is the transconductance extracted from the linear region of the  $I_{ds}$ - $V_{gs}$  curve,  $h$  is the thickness of the SiO<sub>2</sub> layer. Note that  $n$  in eqn (4) is one-dimensional carrier concentration. Therefore the volumetric carrier concentration  $N = n/\pi r^2$ , where  $r$  is nanopillar radius. As a result, the estimated field-effect mobility and carrier concentration of samples B and C are 50.3 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, 6.9 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> and 1.8 × 10<sup>17</sup> cm<sup>-3</sup>, 5.3 × 10<sup>16</sup> cm<sup>-3</sup>, respectively. Meanwhile, the field-effect mobility of sample U can be estimated as ~8.5 × 10<sup>-4</sup> cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> extracted from the shallow slope on the  $I$ - $V_{gs}$  curve corresponding to 1 V  $V_{ds}$ , due to weak n-type behavior. The above results clearly show the effectiveness of *in situ* indium doping on tuning electronic properties of CdS nanopillars.

## 4 Conclusion

CdS is one of the most important optoelectronic materials and its nanostructures can be widely used for a broad spectrum of nanophotonic and nano-optoelectronic applications. However, in order to implement practical applications, the geometry and electrical properties of CdS nanomaterials have to be precisely controlled. In this work, high density CdS nanopillar arrays have been grown inside AAM templates using a catalytic CVD approach, resulting in well aligned nanopillars with highly uniform diameter and length. More importantly, *in situ* indium doping was performed to improve the carrier concentration and field-effect mobility of nanopillars. It was found that indium incorporation in CdS nanopillars changed their growth direction from [211] to [010] due to the change of interfacial energy and surface tension induced by growth guiding channels. And indium source temperature has been found to have a dominant effect on the nanopillar n-type doping level. The electronic properties of the nanopillars have been characterized by configuring them into vertical array devices and field-effect transistors. The measurements showed that conductivity and field-effect mobility of nanopillars can be improved by four and five orders of magnitude, respectively. These results enable future applications of high density array CdS nanopillars for high performance optoelectronic devices.

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